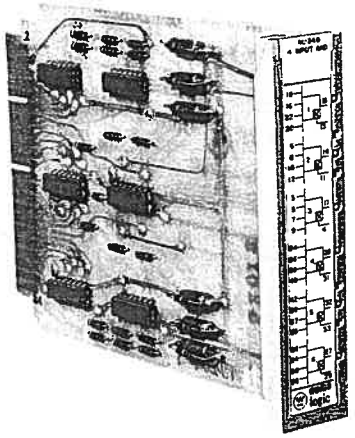
4-INPUT AND
Catalog No. NL-340 & NL-340L



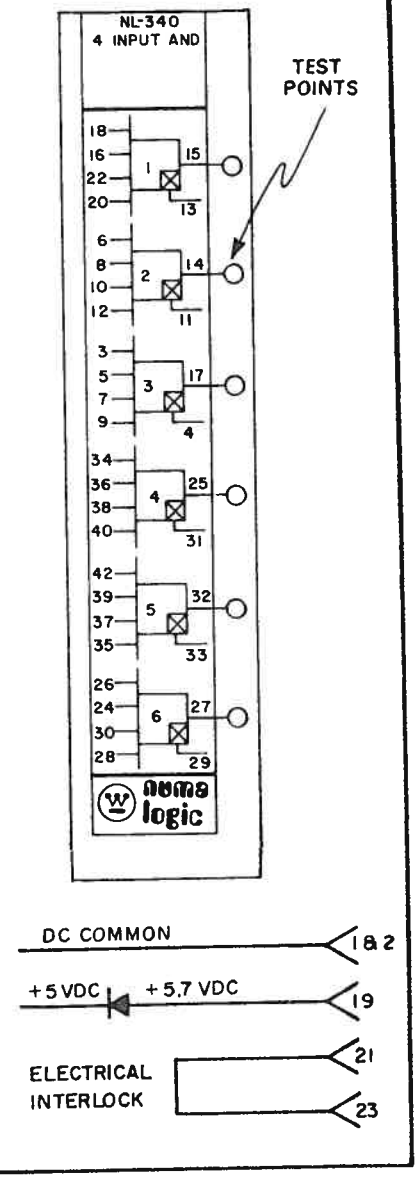
DESCRIPTION

NL-340. Six individual 4-input logic AND gates with TRUE and NOT outputs. No LEDs.
NL-340L. Six individual 4-input logic AND gates with TRUE and NOT outputs. Includes LEDs.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.

SPECIFICATIONS

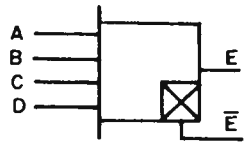
Number of circuits	6
Logic type	TTL
Fan-in (per input)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-340, NL-340L	3 ms, 165 Hz (nominal)
NL-340H, NL-340LH	0.5 ms, 950 Hz (nominal)
NL-340HS, NL-340LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
NL-340 all gates off	100 mA
NL-340 all gates on	70 mA
NL-340L all gates off	100 mA
NL-340L all gates on	130 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 21 & 23
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM

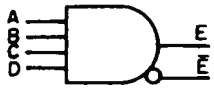


4-INPUT AND

ENGLISH LOGIC SYMBOL



ANSI Y32.14 SYMBOL



TRUTH TABLE

Logic Level Inputs				Logic Level Outputs	
A	B	C	D	E	$\overline{E}$
1	1	1	1	1	0
1	1	1	0	0	1
1	1	0	1	0	1
1	1	0	0	0	1
1	0	1	1	0	1
1	0	1	0	0	1
1	0	0	1	0	1
1	0	0	0	0	1
0	1	1	1	0	1
0	1	1	0	0	1
0	1	0	1	0	1
0	1	0	0	0	1
0	0	1	1	0	1
0	0	1	0	0	1
0	0	0	1	0	1
0	0	0	0	0	1

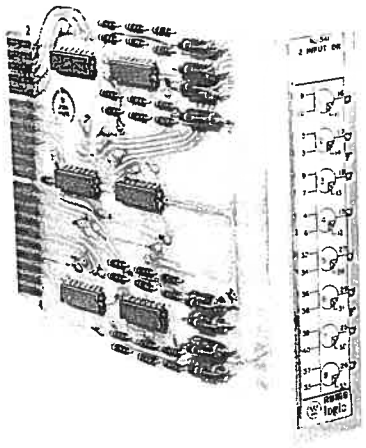
APPLICATION NOTES:

1. Unused AND inputs must be connected to DC common or to one of the circuit's active inputs. Open inputs are logic 0 (broken wire protection).
2. When connecting unused inputs to active inputs do not exceed fan-out (10 unit loads) of previous gate.

2-INPUT OR
Catalog No. NL-341 & NL-341L

DESCRIPTION

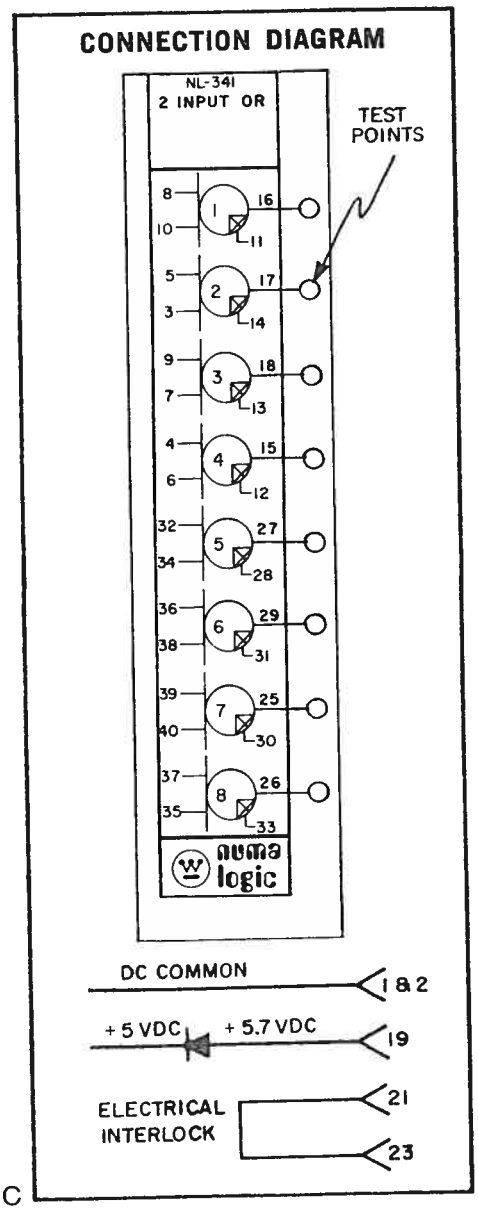
NL-341. Eight individual 2-input logic OR gates with TRUE and NOT outputs. No LEDs.
NL-341L. Eight individual 2-input logic OR gates with TRUE and NOT outputs. Includes LEDs.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



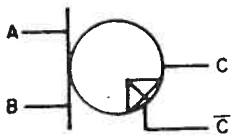
SPECIFICATIONS

Number of circuits	8
Logic type	TTL
Fan-in (per input)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-341, NL-341L	3 ms, 165 Hz (nominal)
NL-341H, NL-341LH	0.5 ms, 950 Hz (nominal)
NL-341HS, NL-341LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
NL-341 all gates off	85 mA
NL-341 all gates on	57 mA
NL-341L all gates off	115 mA
NL-341L all gates on	145 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 23 & 25
Electrical interlock	Pin 21 to pin 23

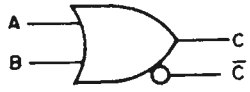
CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL



ANSI Y32.14 SYMBOL



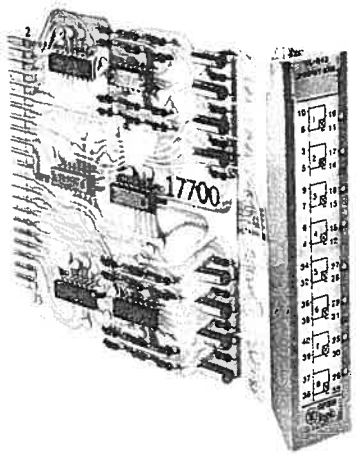
TRUTH TABLE

Logic Level Inputs		Logic Level Outputs	
A	B	C	$\overline{C}$
1	1	1	0
1	0	1	0
0	1	1	0
0	0	0	1

APPLICATION NOTES:

1. Unused OR inputs are logic 0. May be left open or connected to +5.0 VDC

2-INPUT AND
Catalog No. NL-342 & NL-342L



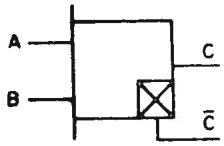
DESCRIPTION

NL-342. Eight individual 2-input logic AND gates with TRUE and NOT outputs. No LEDs.
NL-342L. Eight individual 2-input logic AND gates with TRUE and NOT outputs. Includes LEDs.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.

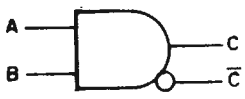
SPECIFICATIONS

Number of circuits	8
Logic type	TTL
Fan-in (per input)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-342, NL-342L	3 ms, 165 Hz (nominal)
NL-342H, NL-342LH	0.5 ms, 950 Hz (nominal)
NL-342HS, NL-342LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
NL-342 all gates off	110 mA
NL-342 all gates on	75 mA
NL-342L all gates off	130 mA
NL-342L all gates on	160 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 25 & 27
Electrical interlock	Pin 21 to pin 23

ENGLISH LOGIC SYMBOL



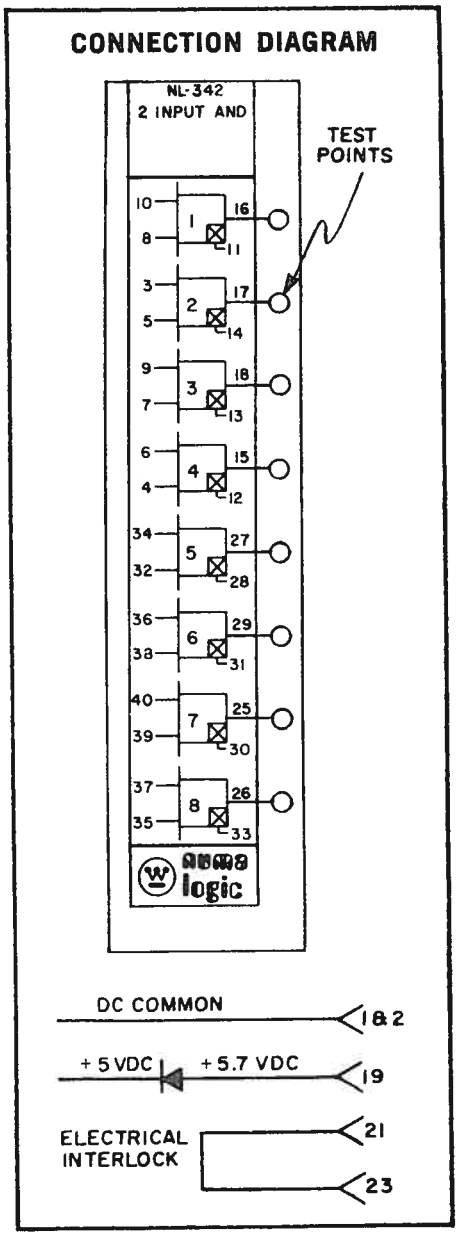
ANSI Y32.14 SYMBOL



TRUTH TABLE

Logic Level Inputs		Logic Level Outputs	
A	B	C	$\bar{C}$
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	1

CONNECTION DIAGRAM

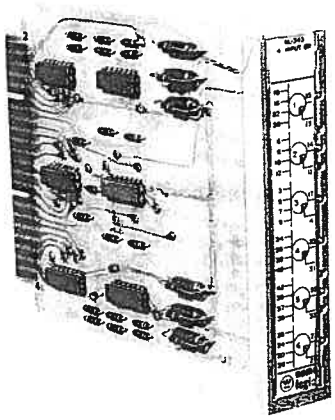


APPLICATION NOTES:

1. Unused AND inputs must be connected to DC common or to the circuit's active input. Open inputs are logic 0 (broken wire protection).
2. When connecting unused input to active input, do not exceed fan-out (10 unit loads) of previous gate.

4-INPUT OR
Catalog No. NL-343 & NL-343L

DESCRIPTION

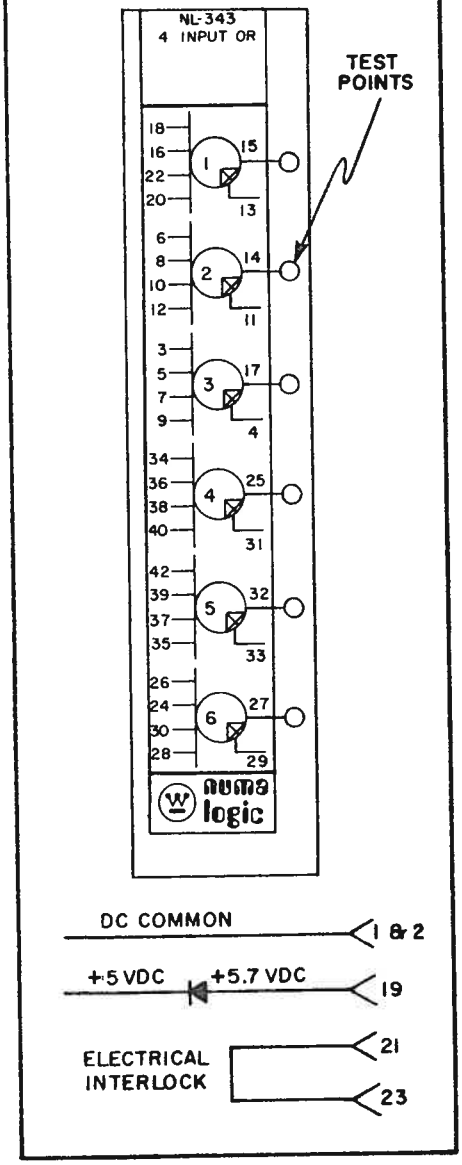


NL-343. Six individual 4-input logic OR gates with TRUE and NOT outputs. No LEDs.
NL-343L. Six individual 4-input logic OR gates with TRUE and NOT outputs. Includes LEDs.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.

SPECIFICATIONS

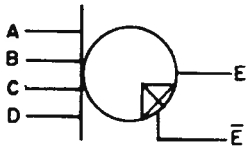
Number of circuits	6
Logic type	TTL
Fan-in (per input)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-343, NL-343L	3 ms, 165 Hz (nominal)
NL-343H, NL-343LH	0.5 ms, 950 Hz (nominal)
NL-343HS, NL-343LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
NL-343 all gates off	40 mA
NL-343 all gates on	55 mA
NL-343L all gates off	55 mA
NL-343L all gates on	110 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 27 & 29
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM

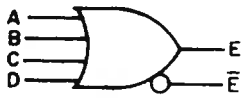


4-INPUT OR

ENGLISH LOGIC SYMBOL



ANSI Y32.14 SYMBOL



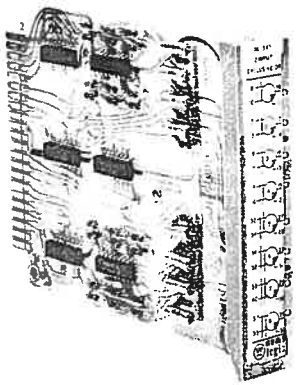
APPLICATION NOTES:

1. Unused OR inputs are logic 0. May be left open or connected to +5.0 VDC.

TRUTH TABLE

Logic Level Inputs				Logic Level Outputs	
A	B	C	D	E	$\overline{E}$
1	1	1	1	1	0
1	1	1	0	1	0
1	1	0	1	1	0
1	1	0	0	1	0
1	0	1	1	1	0
1	0	1	0	1	0
1	0	0	1	1	0
1	0	0	0	1	0
0	1	1	1	1	0
0	1	1	0	1	0
0	1	0	1	1	0
0	1	0	0	1	0
0	0	1	1	1	0
0	0	1	0	1	0
0	0	0	1	1	0
0	0	0	0	0	1

EXCLUSIVE OR
Catalog No. NL-345L



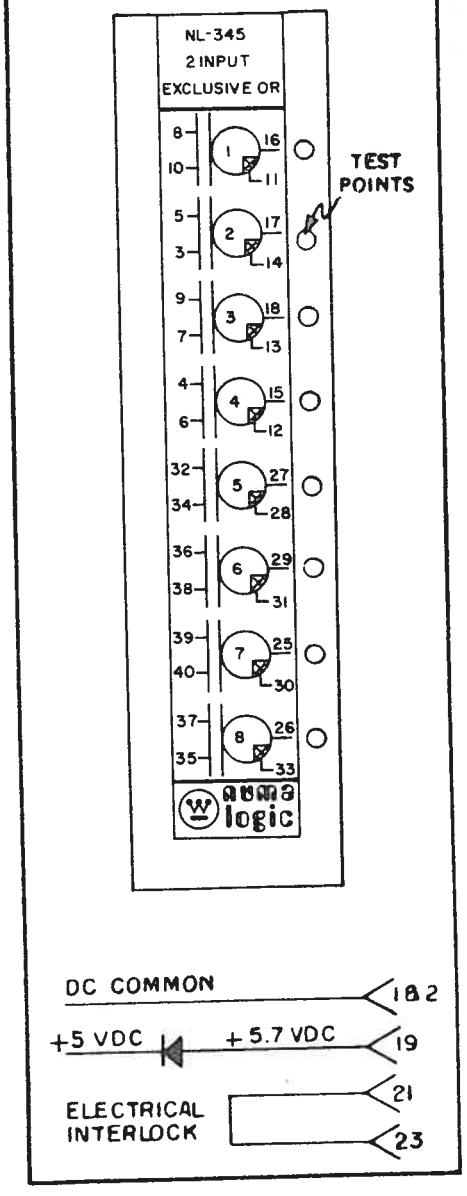
DESCRIPTION

Exclusive OR with TRUE and NOT outputs. LEDs included on TRUE outputs.
PICTORIAL LENS. Standard lens (English logic) shown. Blank lens available for custom marking by user
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.

SPECIFICATIONS

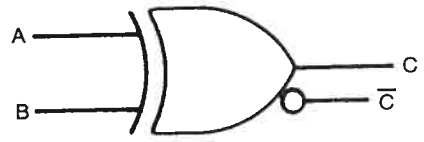
Number of circuits	8
Logic type	TTL
Fan-in (per input)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-345L	3 ms, 165 Hz (nominal)
NL-345LH	0.5 ms, 950 Hz (nominal)
NL-345LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
NL-345L all gates off	193 mA
NL-345L all gates on	245 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 31 & 33
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL

ANSI Y32.14 SYMBOL



TRUTH TABLE

Logic Level Inputs		Logic Level Outputs	
A	B	C	$\overline{C}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

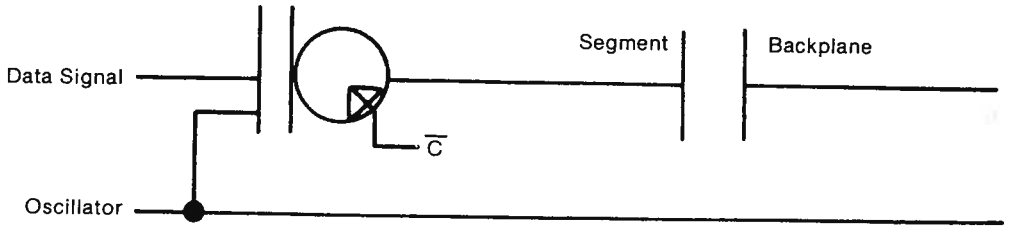
APPLICATION NOTES:

1. When cascading, unused exclusive OR gates must be left open.

EXCLUSIVE OR

APPLICATION EXAMPLES:

1. Driver for Liquid Crystal Displays



If data = 0, then backplane and segment drive are in phase and segment is off.

If data = 1, then backplane and segment drive are out of phase and segment is on.