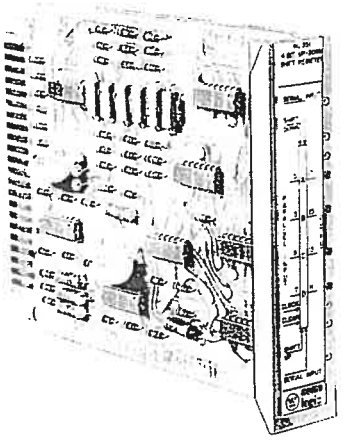
4-BIT UP-DOWN SHIFT REGISTER
Catalog No. NL-351L

DESCRIPTION

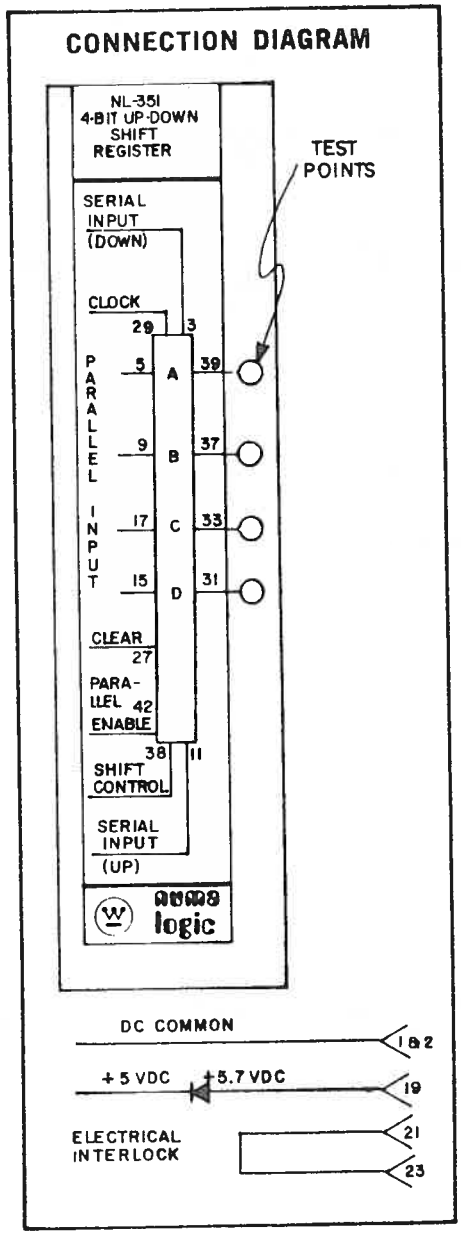
Four stage shift register with series and parallel inputs. Includes LEDs on TRUE outputs. Logic levels are required to select mode (up/down), clock, clear and parallel enable functions.
PICTORIAL LENS. Standard lens (English logic) shown.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



SPECIFICATIONS

Number of circuits	1
Logic type	TTL
Fan-in	
Parallel and serial inputs	
Logic 1	2 unit loads (3.2 mA, source)
Logic 0	2 unit loads (80 microamps, sink)
All other inputs	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-351L	3 ms, 165 Hz (nominal)
NL-351LH	0.5 ms, 950 Hz (nominal)
NL-351LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+ 5.7 ± 0.25 VDC
All stages off	200 mA
All stages on	210 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 23 & 25
Electrical interlock	Pin 21 to pin 23
Control signals	
CLOCK input	10 ms min - pin 29
CLEAR input	10 ms min - pin 27

CONNECTION DIAGRAM



APPLICATION NOTES

1. Contains power-on reset delay circuit (25 ms, nominal).
2. To select SHIFT UP, apply a logic 1 at pin 38. Normal mode with logic 0 is SHIFT DOWN.

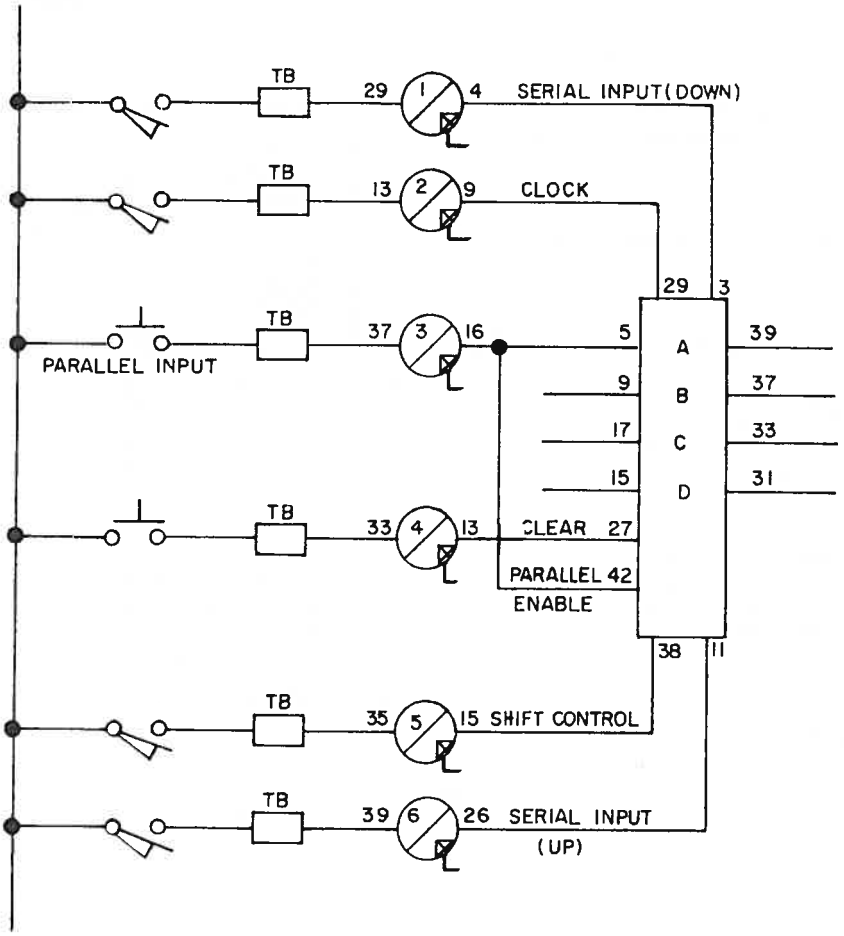
SHIFT CONTROL		
Shift Down	Pin 38	Logic 0
Shift Up	Pin 38	Logic 1

4-BIT UP-DOWN SHIFT REGISTER

3. PARALLEL LOADING. In the parallel load mode, data is loaded into the associated stages and appears at the output after a logic 1 is applied to PARALLEL ENABLE input (pin 42). During parallel loading, serial data flow is inhibited.
4. Serial shift will occur when the clock line transfers from logic 0 to logic 1 (10 ms pulse, min.). Serial input must be present prior to clocking to assure that data is correctly entered.
5. DOWN SHIFT. Apply serial input to pin 3.
   UP SHIFT. Apply serial input to pin 11.
6. CLEAR. All stages are simultaneously set to logic 0 by applying a logic 1 to CLEAR input (pin 27).

APPLICATION EXAMPLES

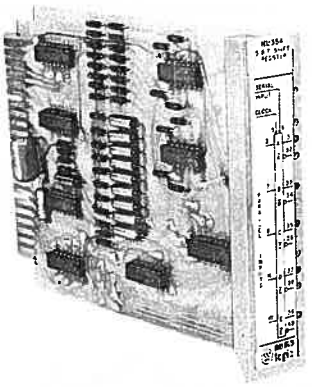
1. Simplified wiring diagram for serial/parallel load.



NOTE: A MANUAL INPUT MAY BE USED TO PRELOAD STAGE A.

IN THIS EXAMPLE, THE MANUAL PARALLEL INPUT IS ALSO USED AS ITS OWN PARALLEL ENABLE. WHEN THE PARALLEL INPUT BUTTON IS DEPRESSED, A LOGIC 1 IS PLACED IN REGISTER A, AND A LOGIC 0 IN REGISTERS B, C & D. UNUSED PARALLEL INPUTS ARE TIED INTERNALLY TO LOGIC 0.

5-BIT SHIFT REGISTER WITH PRESET INPUTS
Catalog No. NL-354L



DESCRIPTION

Five-stage shift register with series and preset inputs and TRUE and NOT outputs. Includes LEDs for each stage.

PICTORIAL LENS. Standard lens (English logic) shown. Blank lens available for custom marking by user.

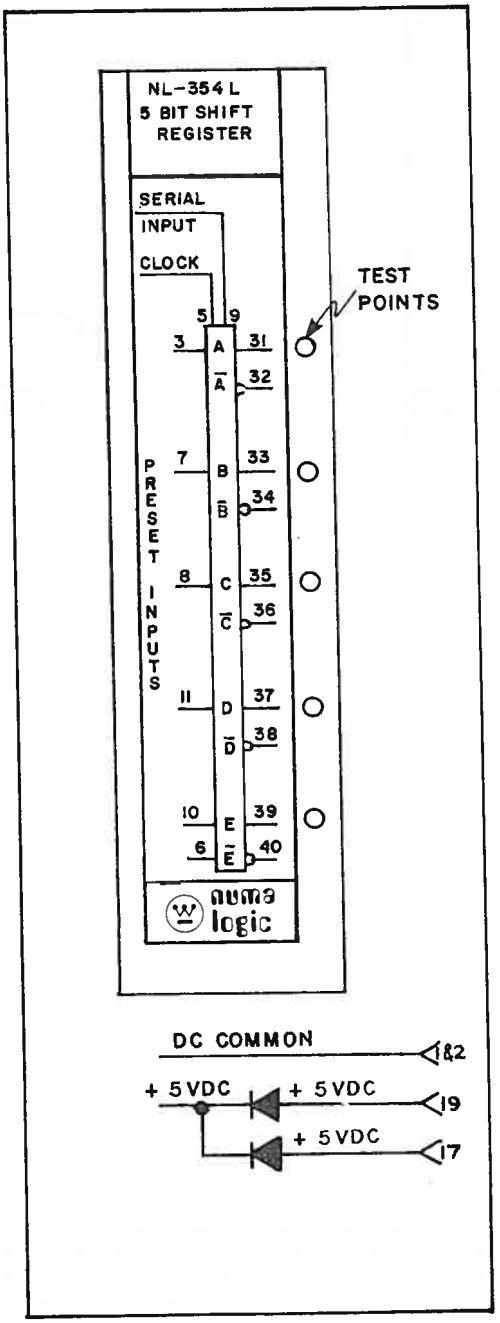
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.

TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.

KEY SLOTS. Prevent incorrect module replacement.

SPECIFICATIONS

Number of circuits	1
Logic type	TTL
Fan-in (per input)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-354L	0.5 ms, 950 Hz (nominal)
NL-354LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+ 5.7 ± 0.25 VDC
All stages off	160 mA
All stages on	170 mA
Temperature rating	0° to 85° C
Noise energy rejection	5 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 31 & 33
Electrical interlock	Pin 21 to pin 23
Control signals	
CLOCK input	1 ms (min.) - pin 5 (500 Hz)
CLEAR input	1 ms (min.) - pin 13



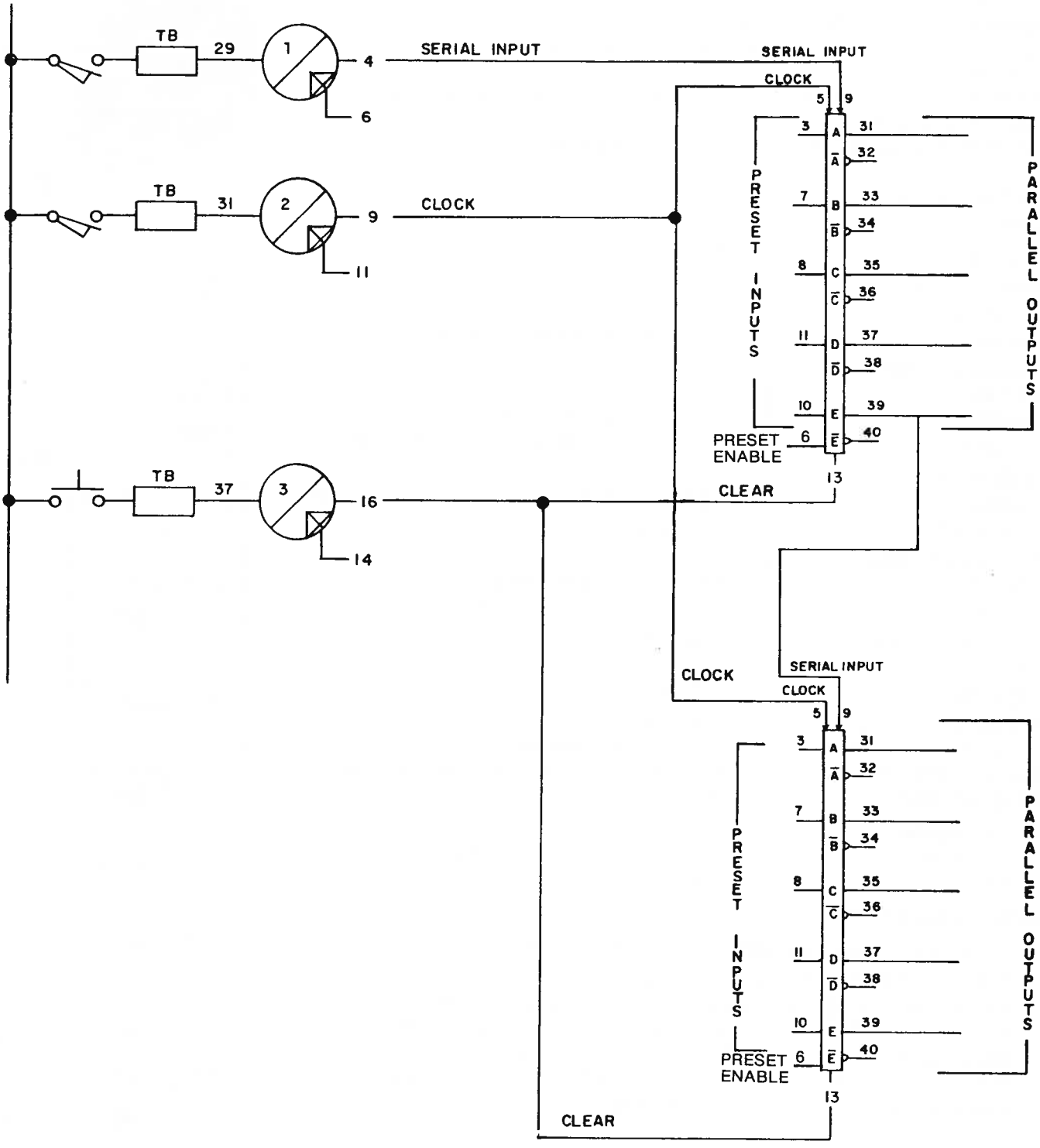
APPLICATION NOTES

1. Contains power-on reset delay circuit (30 ms, nominal).
2. PRESET LOADING. In the preset load mode, data is loaded into the associated stages and appears at the output after a logic 1 is applied to PRESET ENABLE input (pin 6). During preset loading, serial data flow is inhibited. Only a logic 1 can be entered into the shift register through the preset inputs. A logic 0 on the preset inputs will have no effect on the data already loaded into the shift register.
3. Serial shift will occur when the clock line (pin 5) transfers from logic 0 to logic 1 (1 ms pulse). Serial input must be present prior to clocking to assure that data is correctly entered.
4. CLEAR. All stages are simultaneously set to logic 0 by applying logic 1 to CLEAR input (pin 13).

5-BIT SHIFT REGISTER WITH PRESET INPUTS

APPLICATION EXAMPLES

1. Simplified wiring diagram for serial load with expansion to ten bits.



ALL STAGES ARE SIMULTANEOUSLY SET TO THE LOGIC 0 STATE BY APPLYING LOGIC 1 TO THE CLEAR INPUT (PIN 13). THIS CONDITION MAY BE APPLIED INDEPENDENT OF THE STATE OF THE CLOCK INPUT. SERIAL INPUTS MUST BE PRESENT FOR 1 MS (MIN.) FOR DATA TRANSFER. SHIFT OCCURS WHEN THE CLOCK INPUT GOES FROM LOGIC 0 TO LOGIC 1 AND THE CLEAR INPUT IS AT LOGIC 0.