DUAL ADJUSTABLE TIMER — ON/OFF DELAY
Catalog No. NL-344L

DESCRIPTION

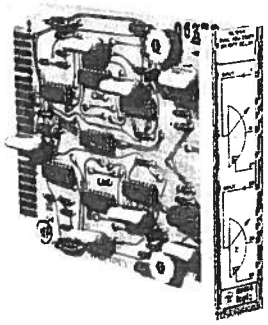
Adjustable timer (200 ms to 15 sec) with timed open and timed closed outputs. Includes LEDs to indicate input and output (TRUE) conditions.

PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.

TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.

TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.

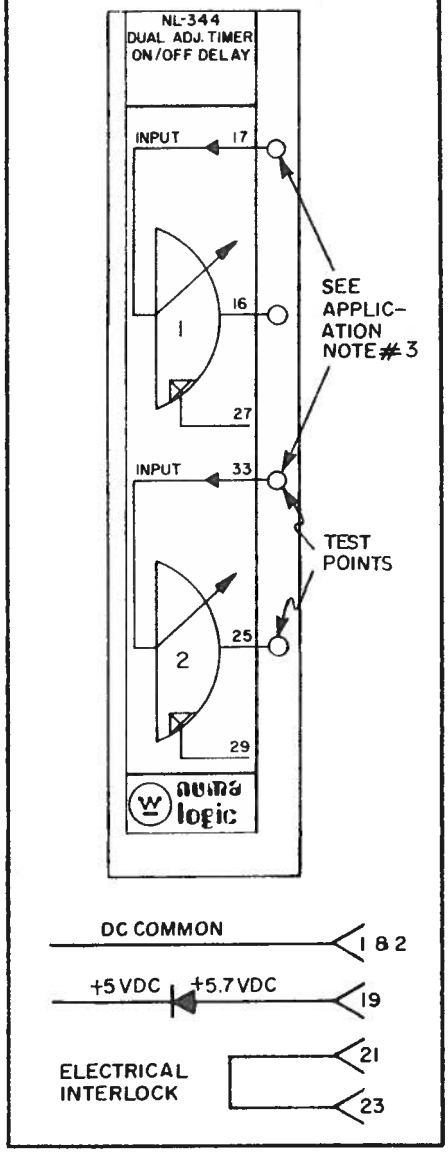
KEY SLOTS. Prevent incorrect module replacement.



SPECIFICATIONS

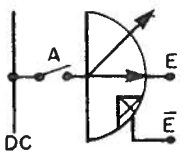
Number of circuits	2
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Timing range	200 ms to 15 sec (adjustable)
Propagation delay	
NL-344L	3 ms, 165 Hz (nominal)
NL-344LH	0.5 ms, 950 Hz (nominal)
NL-344LHS	0.1 ms, 4750 Hz (nominal)
Repeatability	± 1% at constant temperature ± 5% over temperature range
Power requirement	+ 5.7 ± 0.25 VDC
Both timers off	75 mA
Both timers on	125 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 29 & 31
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM

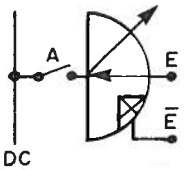


ENGLISH LOGIC SYMBOLS

ADJUSTABLE ON-DELAY TIMER WITH NOT (INVERTED) OUTPUT

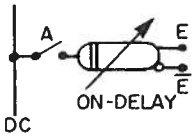


ADJUSTABLE OFF-DELAY TIMER WITH NOT (INVERTED) OUTPUT

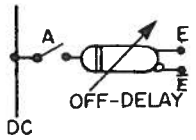


ANSI Y32.14 SYMBOLS

ADJUSTABLE ON-DELAY TIMER WITH INVERTED OUTPUT



ADJUSTABLE OFF-DELAY TIMER WITH INVERTED OUTPUT



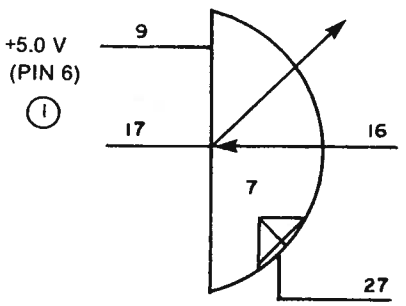
DUAL ADJUSTABLE TIMER — ON/OFF DELAY

APPLICATION NOTES

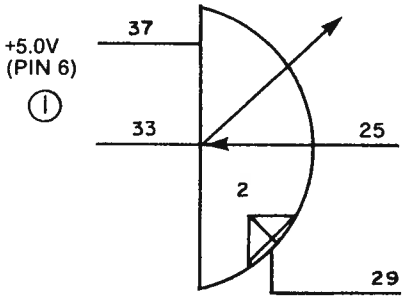
1. Contains power-on reset delay circuit (15 ms, nominal).
2. Both timers are normally on-delay. To convert timer #1 to off-delay, tie pin 9 to pin 6 (+5.0 VDC). To convert timer #2 to off-delay, tie pin 37 to pin 6 (+5.0 VDC).
3. Input test points (pins 17 and 33) may be jumpered to DC common to time out timers.

APPLICATION EXAMPLES

1. Conversion to Off-delay



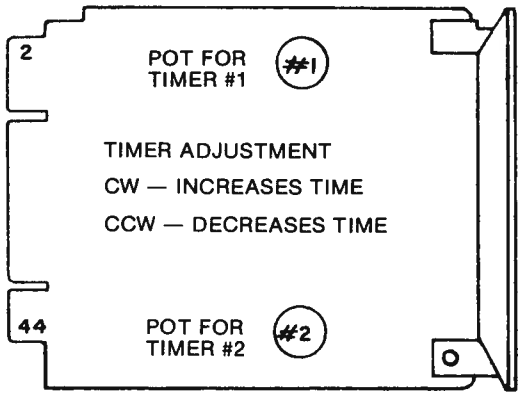
TIMER #1



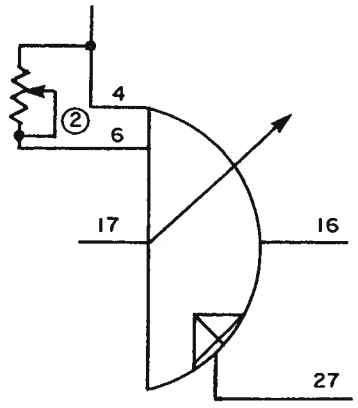
TIMER #2

① WITH PINS 9 AND 37 OPEN, THE RESPECTIVE ELEMENTS ARE AUTOMATICALLY ON-DELAY TIMERS.

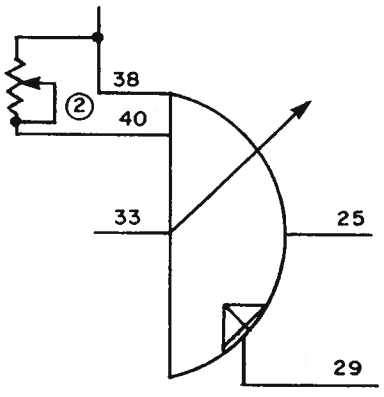
POTENTIOMETER (POT) LOCATIONS
(VIEWED FROM COMPONENT SIDE.)



2. Remote Pot Connection



TIMER #1



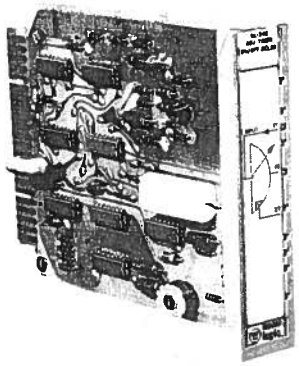
TIMER #2

2. WHEN CONNECTING TO EXTERNAL POT, ADJUST CARD MOUNTED POTENTIOMETER TO THE FULL CW POSITION. A 500K POT IS RECOMMENDED.

ADJUSTABLE TIMER — ON/OFF DELAY
Catalog No. NL-346L

DESCRIPTION

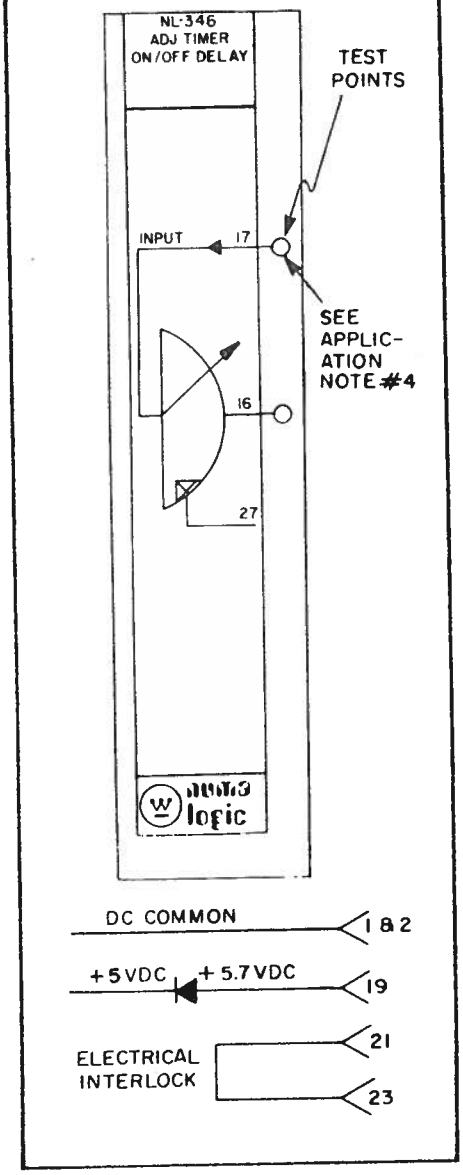
Adjustable timer over three timing ranges (180 ms-3.5 sec, 2-40 sec, 14-300 sec) with timed open and timed closed outputs. Includes LEDs to indicate input and output (TRUE) conditions.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



SPECIFICATIONS

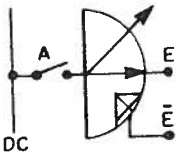
Number of circuits	1
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Timing ranges	See Application Note #2
Propagation delay	
NL-346L	3 ms, 165 Hz (nominal)
NL-346 LH	0.5 ms, 950 Hz (nominal)
NL-346 LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+ 5.7 ± 0.25 VDC
Timer off	115 mA
Timer on	195 mA
Repeatability	± 5% over temperature range ± 0.5% at constant temperature
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 33 & 35
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM

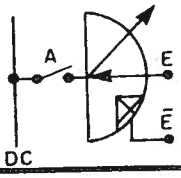


ENGLISH LOGIC SYMBOLS

ADJUSTABLE ON-DELAY TIMER WITH NOT (INVERTED) OUTPUT

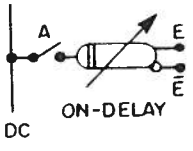


ADJUSTABLE OFF-DELAY TIMER WITH NOT (INVERTED) OUTPUT

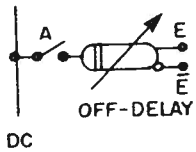


ANSI Y32.14 SYMBOLS

ADJUSTABLE ON-DELAY TIMER WITH INVERTED OUTPUT



ADJUSTABLE OFF-DELAY TIMER WITH INVERTED OUTPUT



ADJUSTABLE TIMER — ON/OFF DELAY

APPLICATION NOTES

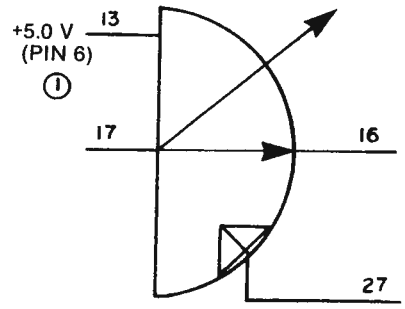
1. Contains power-on reset circuit (15 ms, nominal).
2. Time selection table:

External Wiring	Time	
	Min.	Max.
None required	180 ms	3.5 sec
Tie pin 35 to pin 1	2.0 sec	40 sec
Tie pins 31 & 35 to pin 1	14 sec	300 sec

3. Timer adjustment: To increase setting, rotate potentiometer (pot) clockwise. To decrease setting, rotate pot counter-clockwise.
4. Input test point (pin 17) may be jumpered to DC common to time out timer.

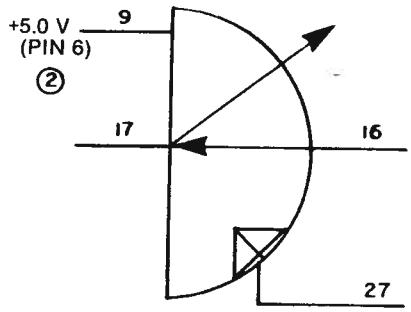
APPLICATION EXAMPLES

1. On-delay Connection



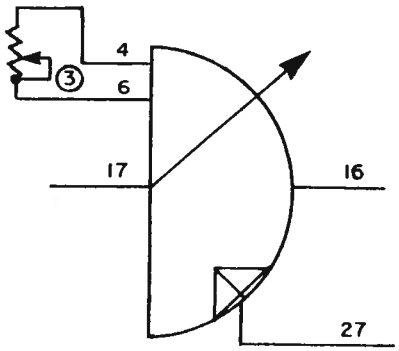
① EXTERNAL WIRING SELECTS ON-DELAY OR OFF-DELAY. FOR ON-DELAY, TIE PIN 13 TO PIN 6.

2. Off-delay Connection



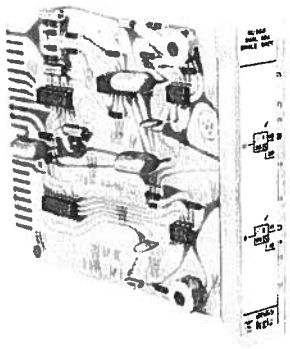
② EXTERNAL WIRING SELECTS ON-DELAY OR OFF-DELAY. FOR OFF-DELAY, TIE PIN 9 to PIN 6.

3. Remote Pot Connection



③ WHEN CONNECTING TO EXTERNAL POT, ADJUST CARD MOUNTED POTENTIOMETER TO FULL CW POSITION. A 500K POT IS RECOMMENDED.

DUAL ADJUSTABLE SINGLE SHOT
Catalog No. NL-350L



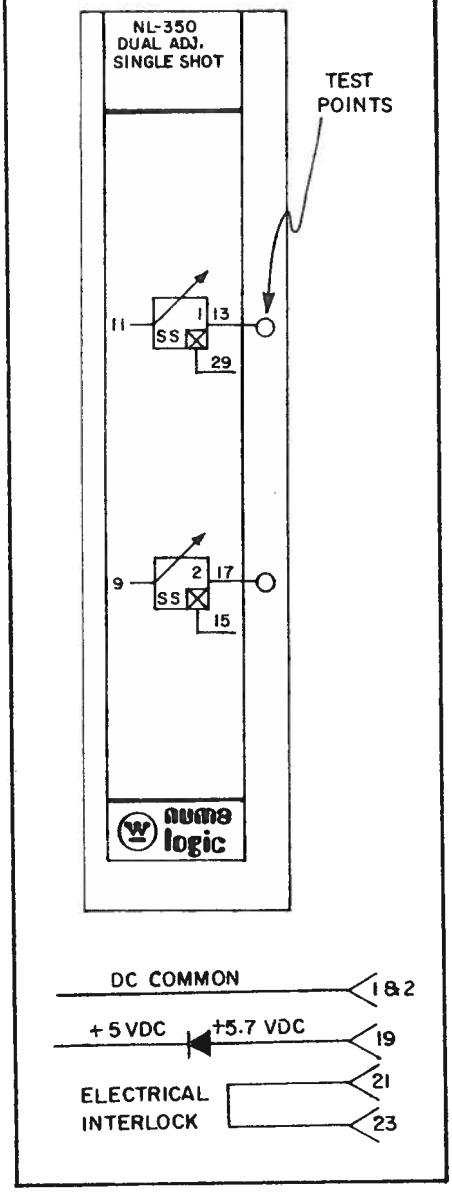
DESCRIPTION

Adjustable single shot with TRUE and NOT outputs (refer to specifications for timing ranges). Includes LEDs. Two circuits.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.

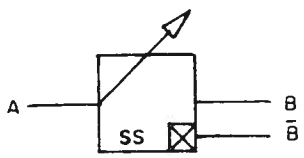
SPECIFICATIONS

Number of circuits	2
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-350L	3 ms, 165 Hz (nominal)
NL-350LH	0.5 ms, 950 Hz (nominal)
NL-350LHS	0.1 ms, 4750 Hz (nominal)
Timing ranges	
NL-350L	10 to 500 ms
NL-350LH	2.5 to 110 ms
NL-350LHS	0.5 to 24 ms
Power requirement	+ 5.7 ± 0.25 VDC, 67 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 21 & 23
Electrical interlock	Pin 21 to pin 23

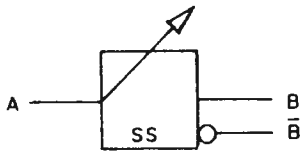
CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL



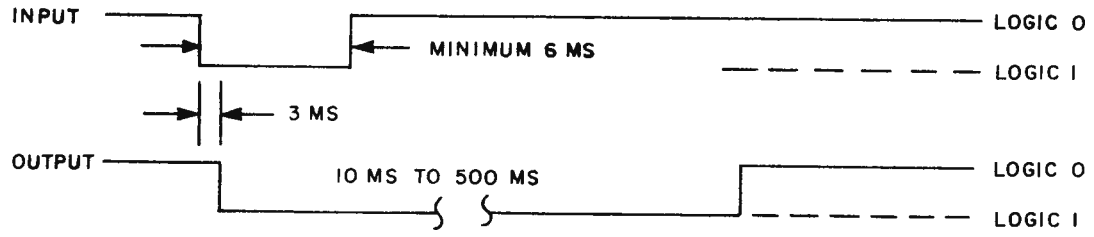
ANSI Y32.14 SYMBOL



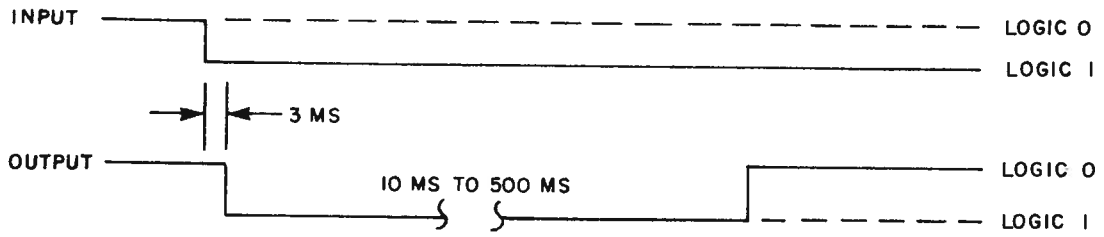
DUAL ADJUSTABLE SINGLE SHOT

APPLICATION NOTES

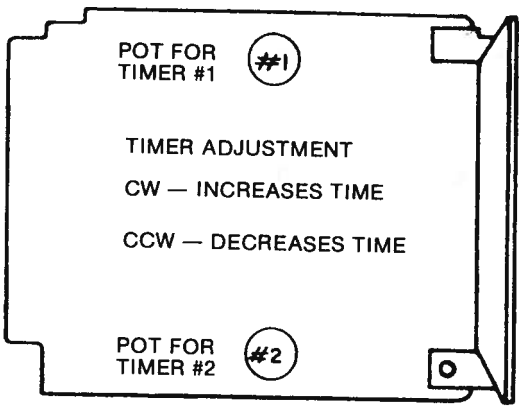
1. Contains power-on reset delay circuit (25 ms, nominal).
2. Timing diagram — output longer than input signal duration.



3. Timing diagram — output shorter than input signal duration.



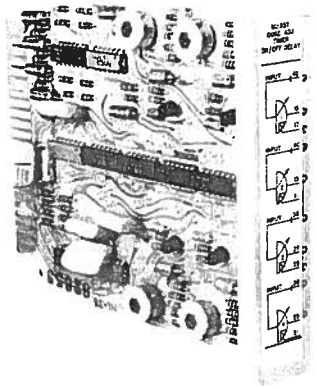
POTENTIOMETER (POT) LOCATIONS (VIEWED FROM COMPONENT SIDE).



QUAD ADJUSTABLE TIMER — ON/OFF DELAY
Catalog No. NL-357L, NL-358L & NL-359L

DESCRIPTION

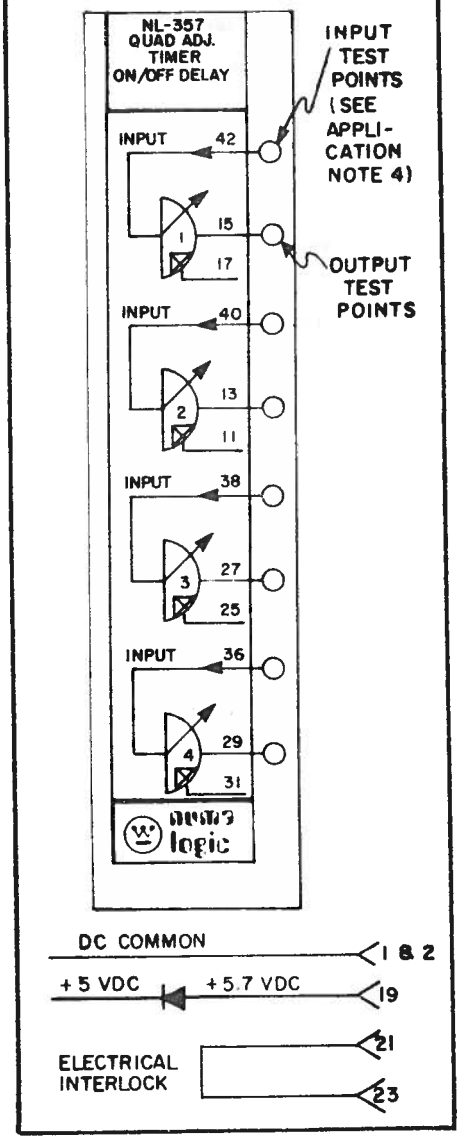
Adjustable timer with timed open and timed closed outputs (refer to specifications for timing ranges). Includes LEDs to indicate input and output (time) conditions. Four circuits.
PICTORIAL LENS. Standard lens (English logic) shown. ANSI Y32.14 lens also available.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



SPECIFICATIONS

Number of circuits	4
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps,source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Repeatability	± 1% at constant temperature ± 5% over temperature range
Reset delay time	3 ms, 165 Hz (nominal)
Timing ranges	
NL-357L	10 ms to 1 sec
NL-358L	50 ms to 5 sec
NL-359L	160 ms to 20 sec
Power requirement	+ 5.7 ± 0.25 VDC
All timers on delay	250 mA
All timers off delay	350 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 35 & 37
Electrical interlock	Pin 21 to pin 23

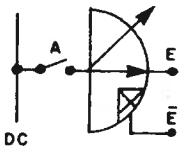
CONNECTION DIAGRAM



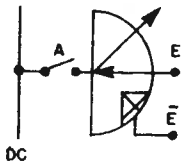
QUAD ADJUSTABLE TIMER — ON/OFF DELAY

ENGLISH LOGIC SYMBOL

ADJUSTABLE ON-DELAY TIMER WITH NOT (INVERTED) OUTPUT

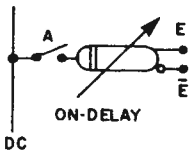


ADJUSTABLE OFF-DELAY TIMER WITH NOT (INVERTED) OUTPUT

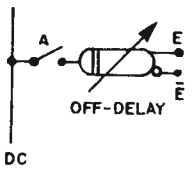


ANSI Y32.14 SYMBOL

ADJUSTABLE ON-DELAY TIMER WITH INVERTED OUTPUT



ADJUSTABLE OFF-DELAY TIMER WITH INVERTED OUTPUT



APPLICATION NOTES

1. Contains power-on reset delay circuit (25 ms, nominal).
2. All timers are internally wired as on delay timers.
3. To convert to off delay timers, wire externally as indicated below:
   - Timer #1 — tie pin 19 to pin 35.
   - Timer #2 — tie pin 19 to pin 33.
   - Timer #3 — tie pin 19 to pin 39.
   - Timer #4 — tie pin 19 to pin 37.
4. Input test points (pins 42, 40, 38 and 36 respectively) may be jumpered to DC common to time out timers.
5. Potentiometer (pot) locations (viewed from component side).