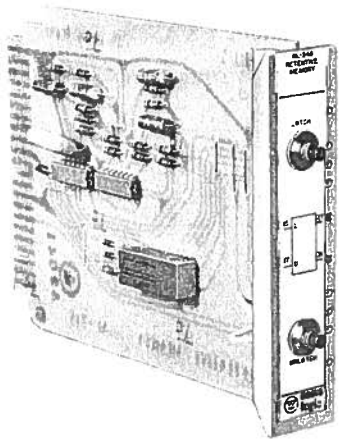
RETENTIVE MEMORY
Catalog No. NL-348L

DESCRIPTION

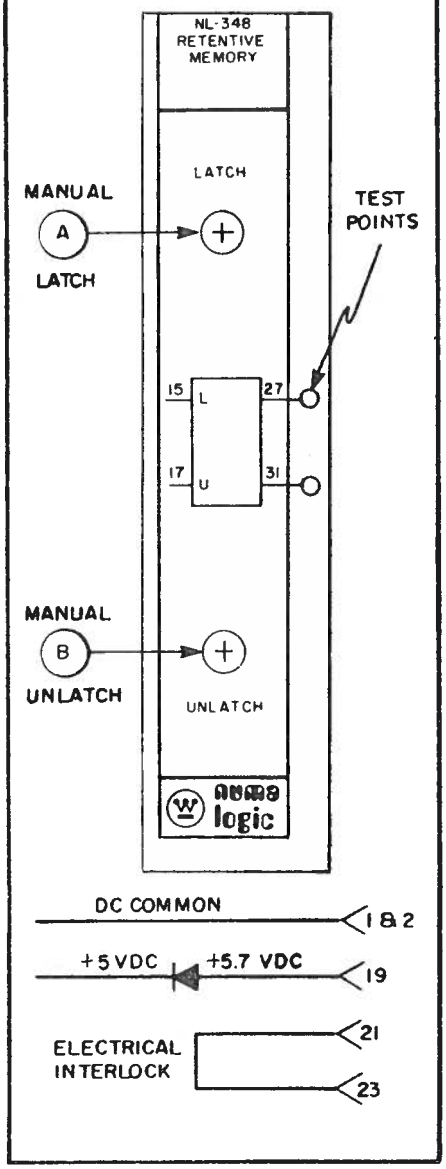
Latch and unlatch functions result from either logic inputs or manual pushbuttons. LEDs indicate output status, which is retained after power interruption.
PICTORIAL LENS. Standard lens (English logic) shown.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



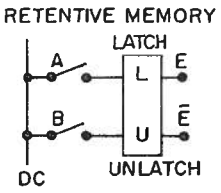
SPECIFICATIONS

Number of circuits	1
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per LATCH or UNLATCH output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-348L	3 ms, 165 Hz (nominal)
NL-348LH	0.5 ms, 950 Hz (nominal)
NL-348LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC, 125 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 9 & 11 and pins 37 & 39
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL



TRUTH TABLE

Inputs				Outputs	
Manual Pushbutton		Logic			
A	B	L	U	E	Ē
1	0	N/A	N/A	1	0
0	1	N/A	N/A	0	1
N/A	N/A	1	0	1	0
N/A	N/A	0	1	0	1
N/A	N/A	1	1	0	1

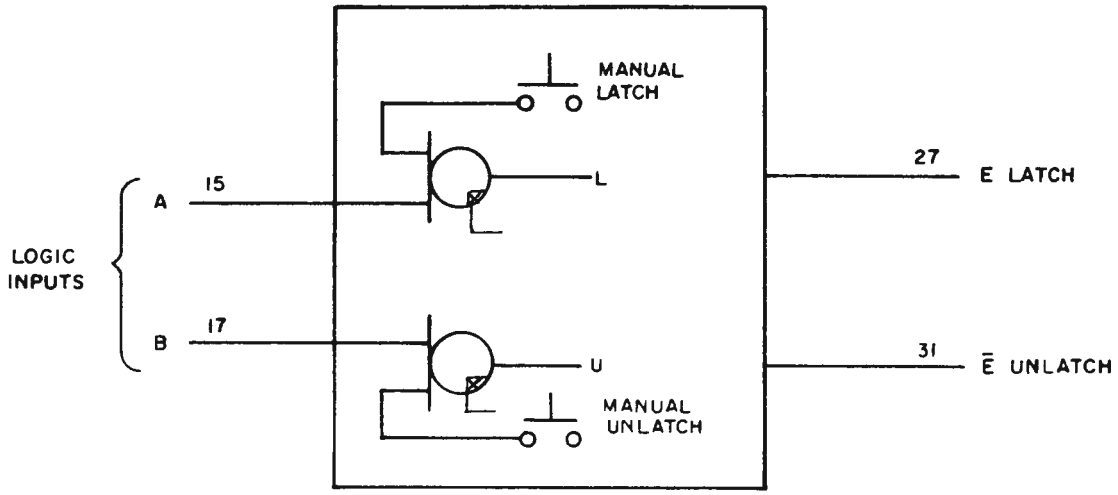
APPLICATION NOTES:

1. Contains power-on reset delay circuit (30 ms, nominal) to prevent change of state during system turn on.
2. Reset signals override set signals.

RETENTIVE MEMORY

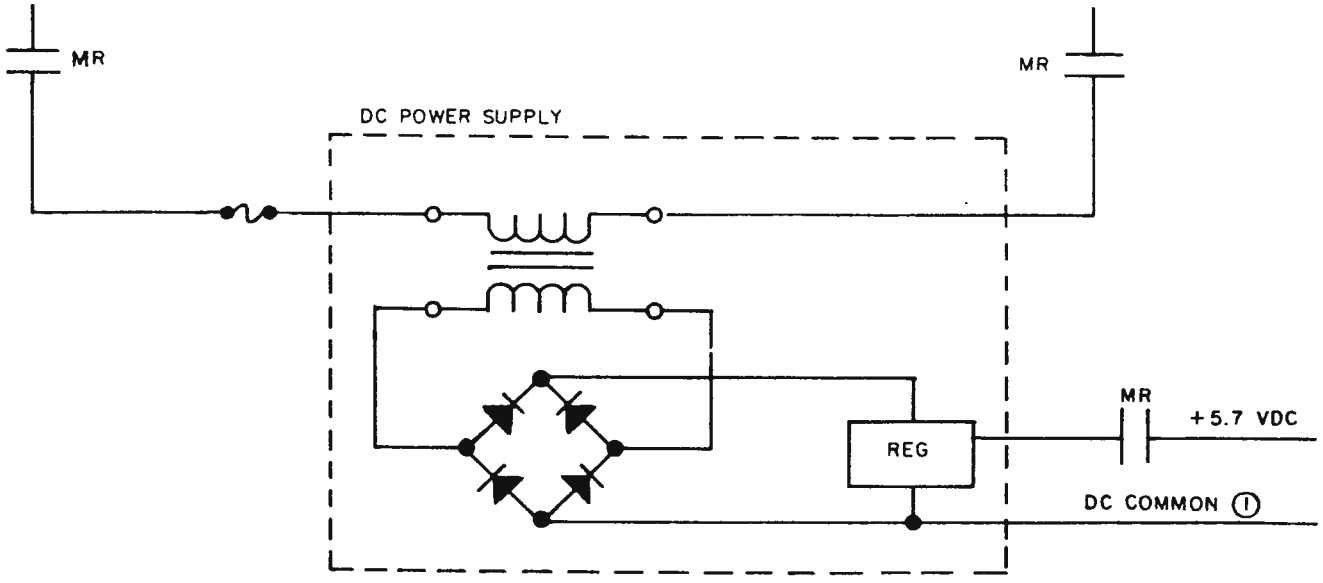
APPLICATION EXAMPLES

1. Connection diagram for logic and manual LATCH and UNLATCH operation.



NOTE: THE MANUAL CONNECTIONS ARE STANDARD AND ARE INTERNAL TO THE MODULE.

2. Simplified wiring diagram for using a master relay in the power supply circuit.
When using an NL-348L, the power supply circuit must contain a normally open contact from a master relay in the B + side. A Master relay is not provided with the power supply.

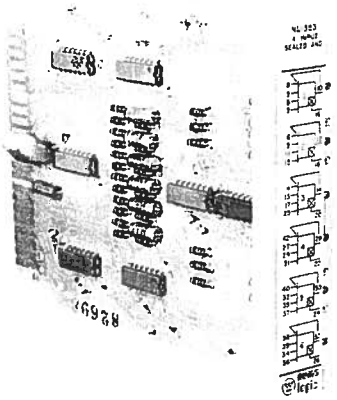


① DO NOT TIE DC COMMON TO PANEL OR EARTH GROUND.

4-INPUT SEALED AND
Catalog No. NL-353L

DESCRIPTION

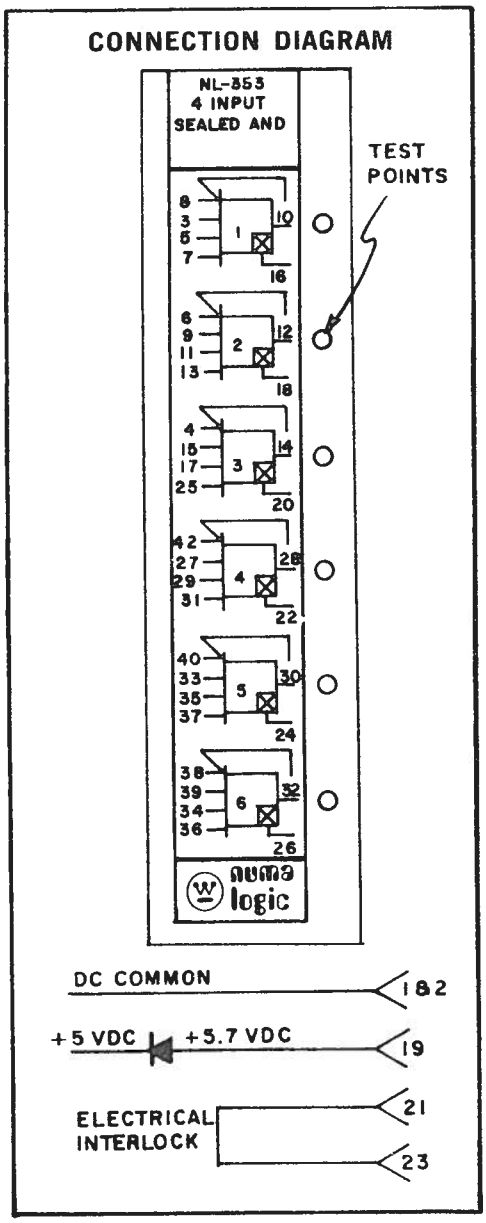
Six individual 4-input sealed AND gates with TRUE and NOT outputs. Includes LEDs on TRUE outputs.
PICTORIAL LENS. Standard lens (English logic) shown.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



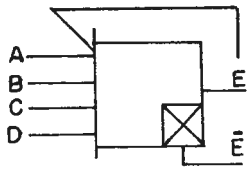
SPECIFICATIONS

Number of circuits	6
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per TRUE or NOT output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-353L	3 ms, 165 Hz (nominal)
NL-353LH	0.5 ms, 950 Hz (nominal)
NL-353LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+ 5.7 ± 0.25 VDC
All gates off	80 mA
All gates on	175 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 27 & 29
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL



TRUTH TABLE

See Application Note No. 4.

4-INPUT SEALED AND

APPLICATION NOTES

1. Contains power-on reset delay circuit (30 ms, nominal).
2. Unused AND inputs must be connected to DC Common or to the active input of the gate. Open inputs are logic 0 (broken wire protection).
3. When connecting unused inputs to active inputs, do not exceed fan-out (10 unit loads) of previous gate.
4. The NL-353L consists of an AND gate requiring that all inputs be at logic 1 to establish a logic 1 at the output. Input A consists of a 2-input OR gate (Fig. 1). Once the AND gate is activated, the logic 1 at A may be removed. Removal of logic 1 from B, C or D inputs will disqualify the output at E.

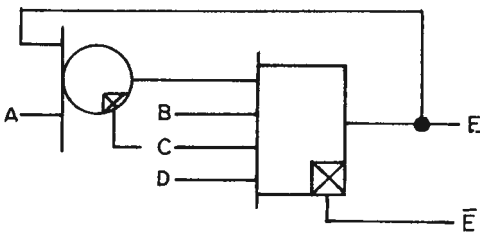
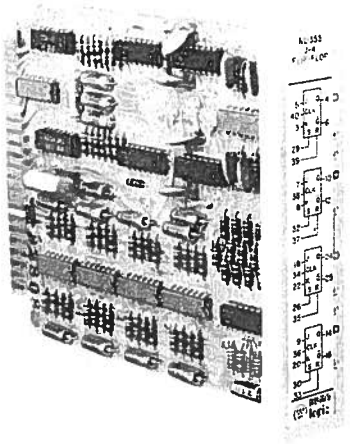


Fig 1. Sealed AND equivalent logic circuit.

J - K FLIP-FLOP
Catalog No. NL-355L

DESCRIPTION

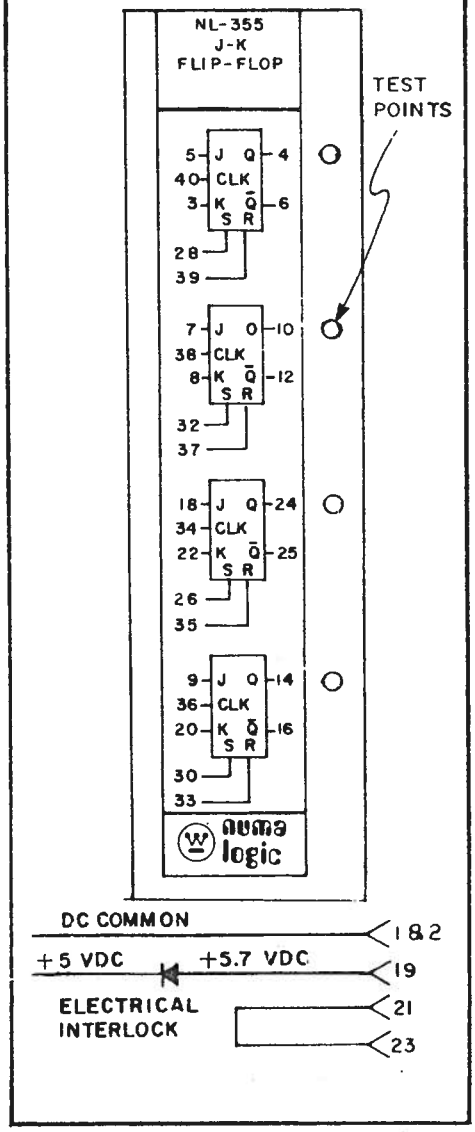
Four J - K Flip-Flop circuits. Includes LEDs to indicate when Q output is TRUE.
PICTORIAL LENS. Standard lens (English logic) shown.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



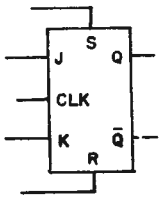
SPECIFICATIONS

Number of circuits	4
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per Q or $\overline{Q}$ output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-355L	0.5 ms, 950 Hz (nominal)
NL-355LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ±0.25 VDC
All flip-flops set	180 mA
All flip-flops reset	175 mA
Temperature rating	0° to 85° C
Noise energy rejection	4 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 29 & 31
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL



TRUTH TABLE

S	R	J	K	CLK	Q	$\overline{Q}$
1	0	X	X	X	1	0
0	1	X	X	X	0	1
1	1	X	X	X	0	1
0	0	0	0	↓	Q	$\overline{Q}$
0	0	0	1	↓	0	1
0	0	1	0	↓	1	0
0	0	1	1	↓	$\overline{Q}$	Q

X = EITHER 1 or 0

↓ = TRANSITION FROM LOGIC 0 TO LOGIC 1

RESET WILL OVERRIDE SET, CLK, J&K

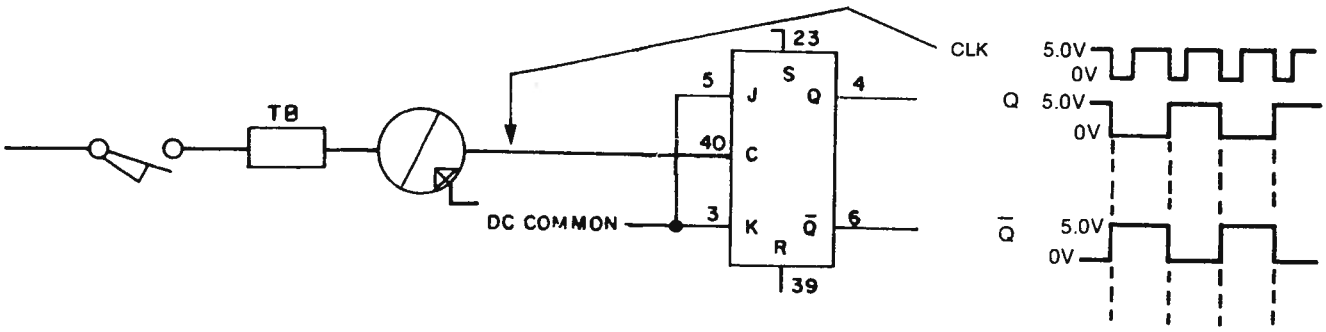
DESIRED INFORMATION MUST BE PRESENT AT J&K BEFORE CLOCK BECOMES TRUE (LOGIC 1). Q STATES CHANGE ACCORDING TO TRUTH TABLE WHEN CLOCK BECOMES TRUE (↓).

APPLICATION NOTES

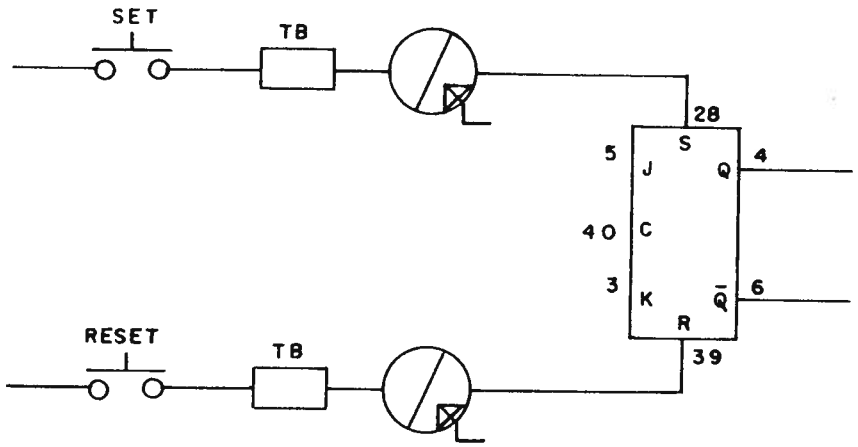
1. Contains power-on reset delay circuit (30 ms, nominal).
2. Clocks on transition from a logic 0 to a logic 1.

APPLICATION EXAMPLES

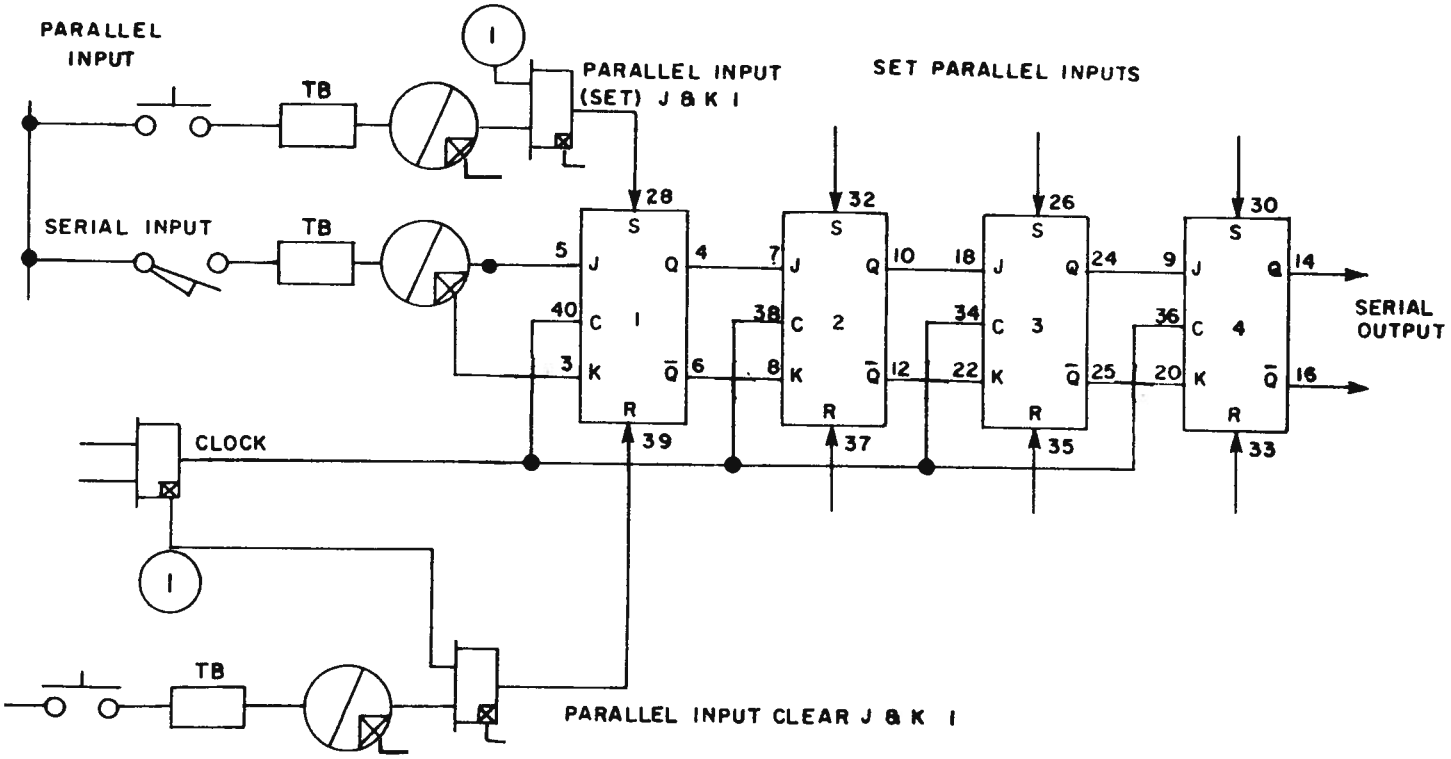
1. Wiring diagram for a Toggle Flip-Flop



2. Wiring diagram for a Set and Reset Flip-Flop

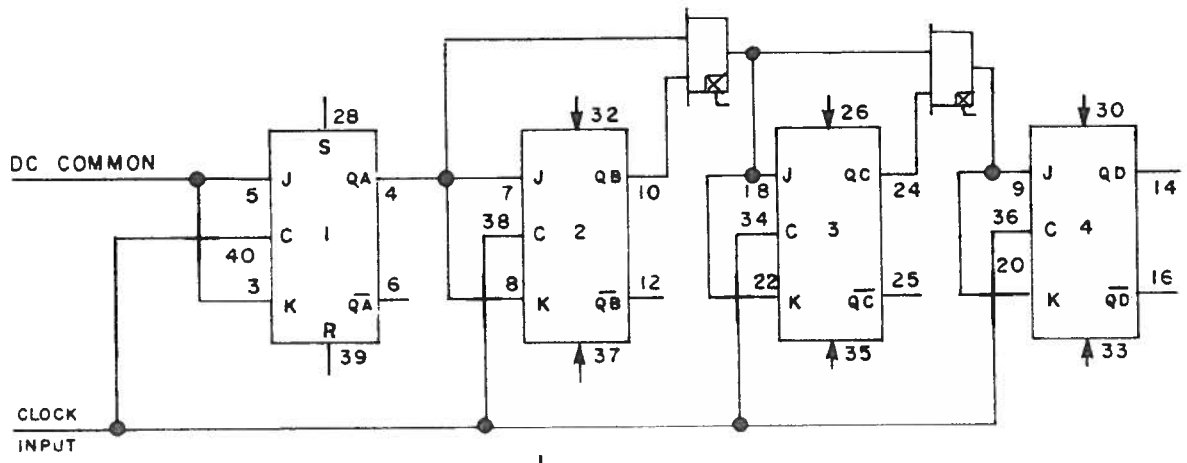


3. Wiring diagram for a 4-bit Stage Shift with Parallel Inputs



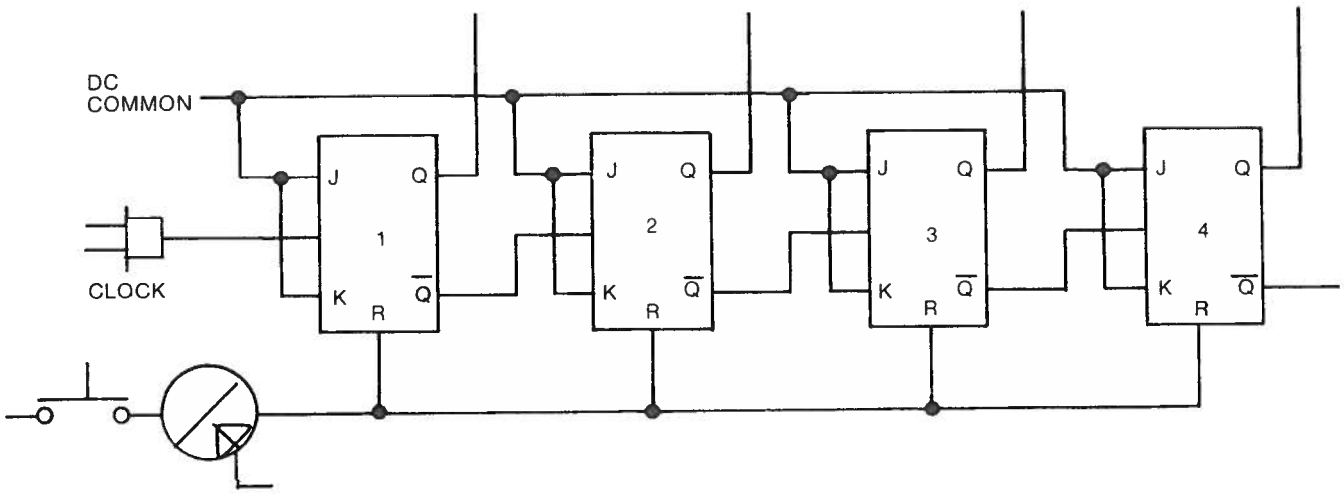
APPLICATION EXAMPLES

4. Wiring diagram for a 4-stage Synchronous Binary Counter

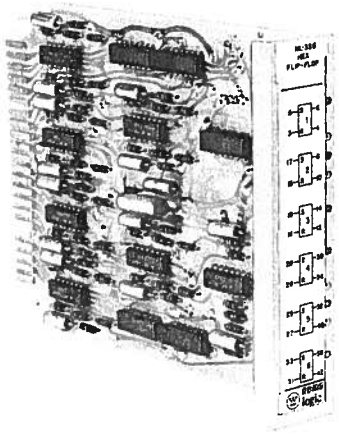


State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

5. Wiring digram for a binary ripple counter:
   a.) tie all J & K inputs to DC Common;
   b.) tie the external clock to the first stage clock input.
   c.) clock successive stages from the $\overline{Q}$ output of the previous stage.



HEX SR FLIP-FLOP
Catalog No. NL-356L



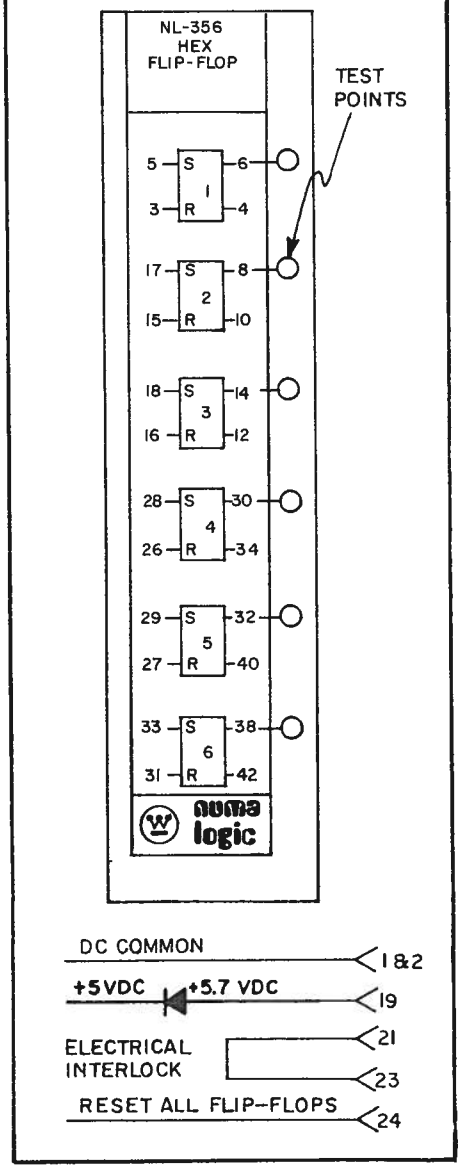
DESCRIPTION

Set-reset flip-flop. Includes LEDs to indicate when outputs are set. Six circuits.
PICTORIAL LENS. Standard lens (English logic) shown.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.

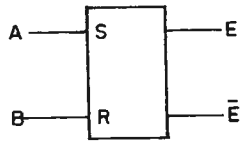
SPECIFICATIONS

Number of circuits	6
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-356L	3 ms, 165 Hz (nominal)
NL-356LH	0.5 ms, 950 Hz (nominal)
NL-356LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
All flip-flops set	230 mA
All flip-flops reset	140 mA
Temperature rating	0° to 85° C
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 11 & 13 and pins 33 & 35
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



ENGLISH LOGIC SYMBOL



TRUTH TABLE

Inputs - DC		Outputs - DC	
A	B	E	$\bar{E}$
1	0	1	0
0	1	0	1
1	1	0	1

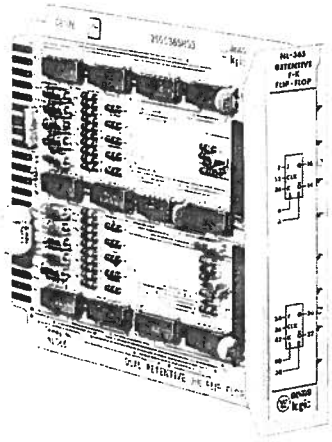
APPLICATION NOTES:

1. Contains power-on reset delay circuit (30 ms, nominal).
2. Reset input overrides set.
3. Logic 1 applied at pin 24 resets all flip-flops.
4. On power-up with no input at A, output $\bar{E}$ will be at logic 1.

RETENTIVE J-K FLIP-FLOP
Catalog No. NL-365L

DESCRIPTION

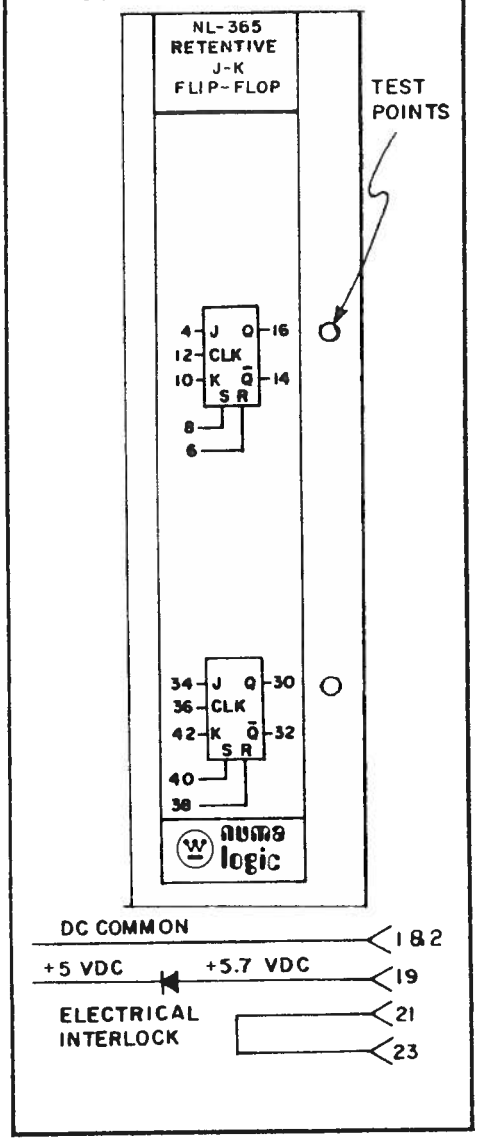
Two retentive J-K Flip-Flop circuits. Includes LEDs to indicate when Q outputs are TRUE.
PICTORIAL LENS. Standard lens (English logic) shown.
TEST POINTS. All TRUE outputs are accessible at front faceplate to facilitate signal tracing.
TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.
KEY SLOTS. Prevent incorrect module replacement.



SPECIFICATIONS

Number of circuits	2
Logic type	TTL
Fan-in	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out (per Q or $\overline{Q}$ output)	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	
NL-365L	0.5 ms, 950 Hz (nominal)
NL-365LHS	0.1 ms, 4750 Hz (nominal)
Power requirement	+5.7 ± 0.25 VDC
All flip-flops set	200 mA
All flip-flops reset	110 mA
Temperature rating	0° to 85°C
Noise energy rejection	4 x 10^{-6} watt seconds
Mechanical keying	Between pins 13 & 15 and pins 31 & 33
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



TRUTH TABLE

S	R	J	K	CLK	Q	$\overline{Q}$
1	0	X	X	X	1	0
0	1	X	X	X	0	1
1	1	X	X	X	0	1
0	0	0	0	↓	Q	$\overline{Q}$
0	0	0	1	↓	0	1
0	0	1	0	↓	1	0
0	0	1	1	↓	$\overline{Q}$	Q

X = either 1 or 0

↓ = transition from logic 0 to logic 1

Reset will override Set, CLK, J & K

Desired information must be present at J & K before clock becomes TRUE (logic 1). Q states change according to truth table when clock becomes TRUE (↓).

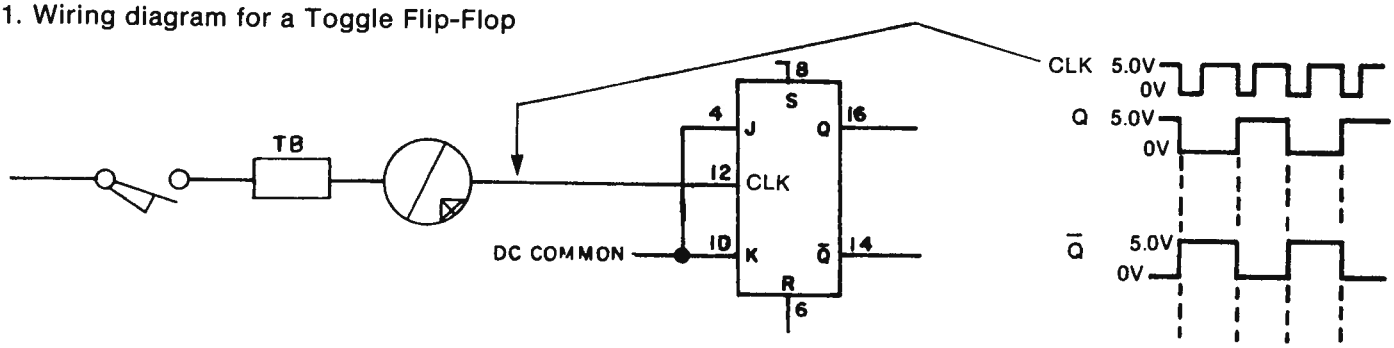
RETENTIVE J-K FLIP-FLOP

APPLICATION NOTES

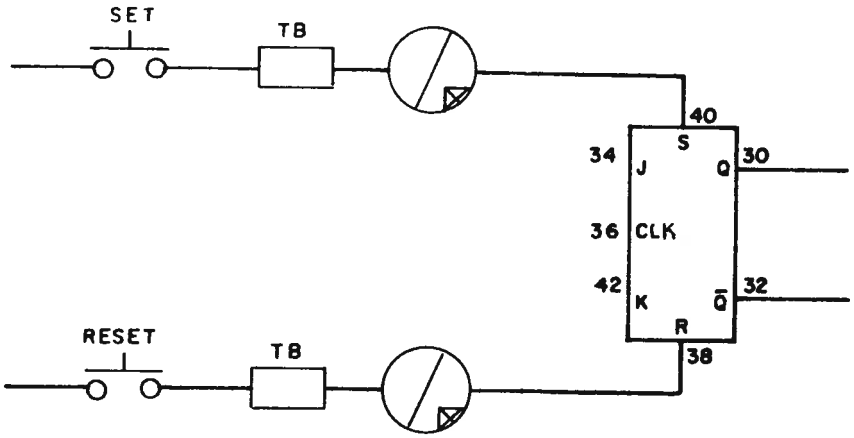
1. When AC power is turned off, the DC power supply can stay above 4.5V from 10 to 70 milliseconds. The logic system and NL-365L will remain operational during this time and care must be taken to determine the effect this might have on the NL-365L inputs after power down, especially if these inputs are driven off of the NOT side of the input interfacing logic. It may be necessary to break 5.7 VDC at power down (see page G2, Note 2).
2. Clocks on transition from logic 0 to a logic 1 (↑).

APPLICATION EXAMPLES

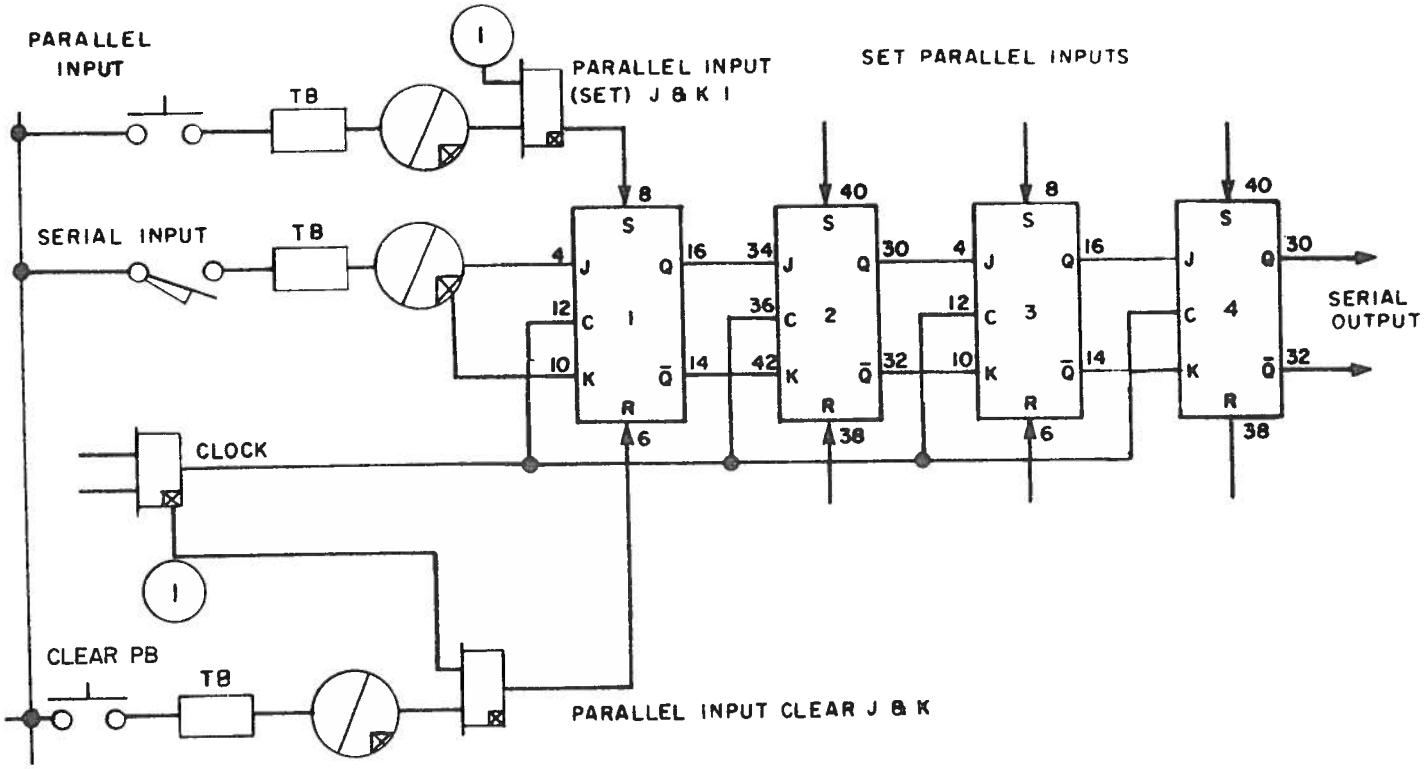
1. Wiring diagram for a Toggle Flip-Flop



2. Wiring diagram for a Set and Reset Flip-Flop



3. Wiring diagram for a 4-bit Stage Shift with Parallel Inputs



EPROM MODULE
Catalog Nos. NL-368 and NL-368A

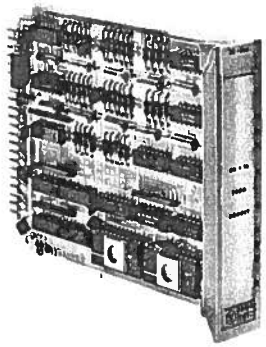
DESCRIPTION

Erasable Programmable Read-Only Memory module with 2048, 16-bit words of memory. May be addressed externally or with an on-board counter. Operates between 0°C (32°F) and 70°C (158°F). Factory programming available.

PICTORIAL LENS. Standard lens shown. Blank lens available for custom marking by user.

TERMINATION. Nickel gold-plated edge pins are used for all input-output connections.

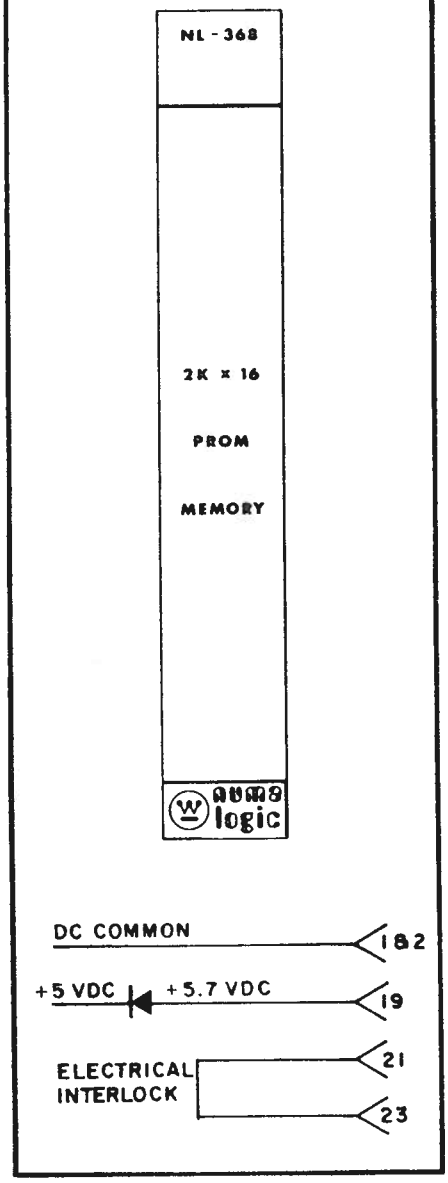
KEY SLOTS. Prevent incorrect module replacement.



SPECIFICATIONS

Number of circuits	1
Logic type	TTL
Fan-in (for preset data inputs, clear, count up, count down, preset and enable)	
Logic 1	2 unit loads (3.2 mA, source)
Logic 0	2 unit loads (80 microamps, sink)
Fan-in (for address inputs A0 — A10)	
Logic 1	1 unit load (1.6 mA, source)
Logic 0	1 unit load (40 microamps, sink)
Fan-out	
Logic 1	10 unit loads (16 mA, sink)
Logic 0	10 unit loads (400 microamps, source)
Logic levels	
Logic 1	0.0 to 0.8 VDC (nominal)
Logic 0	2.4 to 5.0 VDC (nominal)
Propagation delay	3 ms (for preset data inputs, clear, count up, count down, preset and enable)
Power requirements	+5.7 VDC ± 0.25 VDC 400 mA (NL-368) 840 mA (NL-368A)
Temperature rating	0° to 70°C (32°C to 158°F)
Noise energy rejection	25 x 10^{-6} watt seconds
Mechanical keying	Between pins 14 & 16 and pins 38 & 40
Electrical interlock	Pin 21 to pin 23

CONNECTION DIAGRAM



EPROM MODULE

TABLE FOR PRESET DATA INPUTS A7 — A10

PRESET DATA INPUTS

Binary Weight	1024	512	256	128
NL-368 Pin #	3	4	5	6
NL-368 Label	A10	A9	A8	A7
Step Number				
0000	0	0	0	0
0128	0	0	0	1
0256	0	0	1	0
0384	0	0	1	1
0512	0	1	0	0
0640	0	1	0	1
0768	0	1	1	0
0896	0	1	1	1
1024	1	0	0	0
1152	1	0	0	1
1280	1	0	1	0
1408	1	0	1	1
1536	1	1	0	0
1664	1	1	0	1
1792	1	1	1	0
1920	1	1	1	1

1. A0 — A6 ARE TIED INTERNALLY TO LOGIC 0 OF THE EPROM MEMORY CHIP (LOGIC 0 = 0.0 VDC). THEY ARE NOT ATTACHED TO THE EDGE CONNECTOR PINS.
2. PRESET DATA INPUTS ARE USED ONLY WHEN THE PRESET INPUT IS AT LOGIC 1.
3. ONLY THE "NOT" OUTPUTS OF THE COUNTER ARE ATTACHED TO THE EDGE CONNECTOR PINS. THE LOGIC LEVELS FOR THESE "NOT" OUTPUTS WILL BE THE INVERSE OF THE LOGIC LEVELS FOR THE PRESET DATA INPUTS.

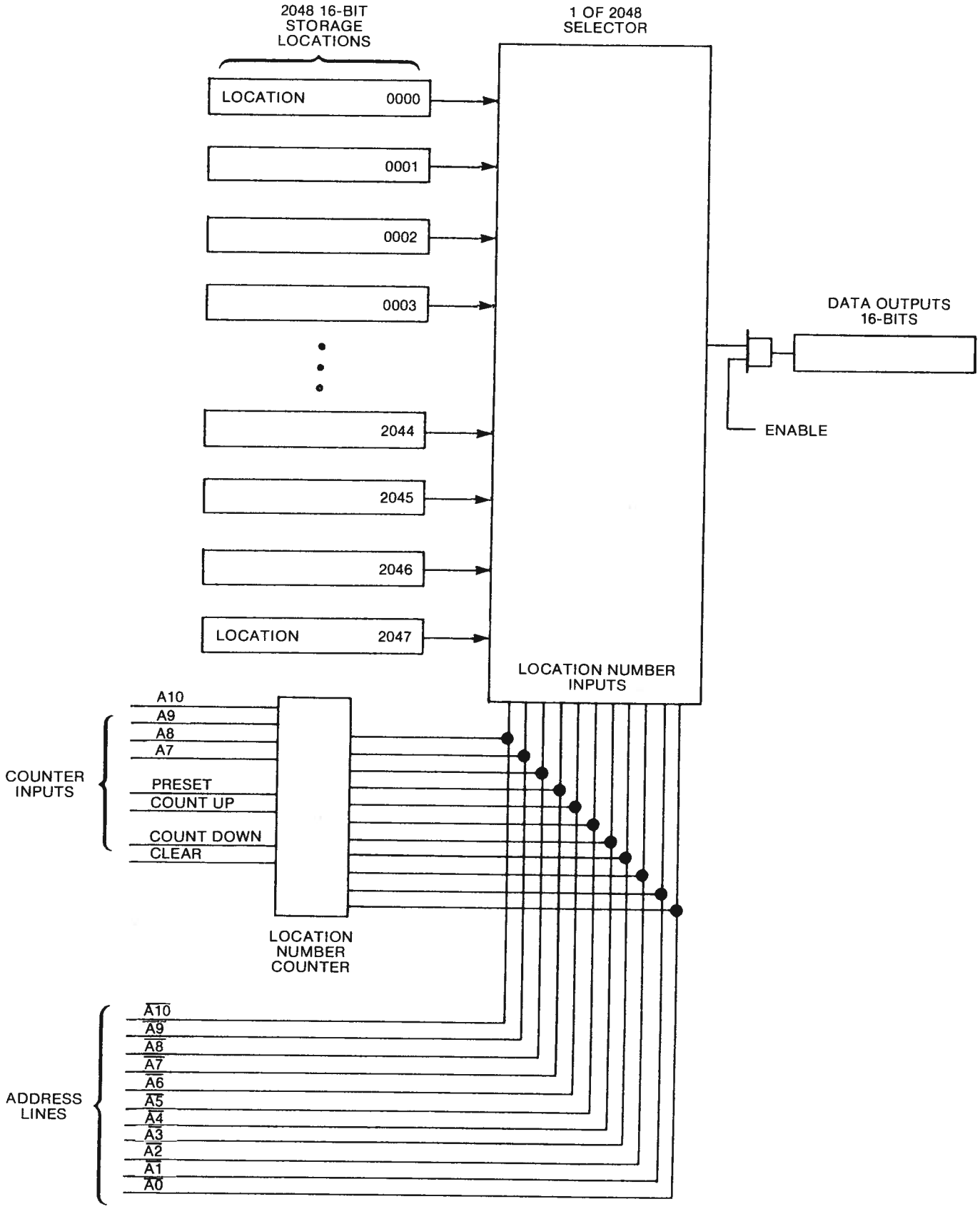
TABLE FOR ADDRESS INPUTS $\overline{A0} \rightarrow \overline{A10}$

	ADDRESS INPUTS $\overline{A0} \rightarrow \overline{A10}$																					
	VOLTAGE LEVELS											LOGIC LEVELS										
Location No.	$\overline{A10}$ — 1024	$\overline{A9}$ — 512	$\overline{A8}$ — 256	$\overline{A7}$ — 128	$\overline{A6}$ — 64	$\overline{A5}$ — 32	$\overline{A4}$ — 16	$\overline{A3}$ — 8	$\overline{A2}$ — 4	$\overline{A1}$ — 2	$\overline{A0}$ — 1	$\overline{A10}$ — 1024	$\overline{A9}$ — 512	$\overline{A8}$ — 256	$\overline{A7}$ — 128	$\overline{A6}$ — 64	$\overline{A5}$ — 32	$\overline{A4}$ — 16	$\overline{A3}$ — 8	$\overline{A2}$ — 4	$\overline{A1}$ — 2	$\overline{A0}$ — 1
0000	L	L	L	L	L	L	L	L	L	L	L	1	1	1	1	1	1	1	1	1	1	1
0001	L	L	L	L	L	L	L	L	L	L	H	1	1	1	1	1	1	1	1	1	1	0
0002	L	L	L	L	L	L	L	L	L	H	L	1	1	1	1	1	1	1	1	1	0	1
0003 etc.	L	L	L	L	L	L	L	L	L	H	H	1	1	1	1	1	1	1	1	1	0	0
0100	L	L	L	L	H	H	L	L	H	L	L	1	1	1	1	0	0	1	1	0	1	1
0101 etc.	L	L	L	L	H	H	L	L	H	L	H	1	1	1	1	0	0	1	1	0	1	0
2046	H	H	H	H	H	H	H	H	H	H	L	0	0	0	0	0	0	0	0	0	0	1
2047	H	H	H	H	H	H	H	H	H	H	H	0	0	0	0	0	0	0	0	0	0	0

H = 2.4 — 5.0 VDC = logic 0
L = 0.0 — 0.8 VDC = logic 1

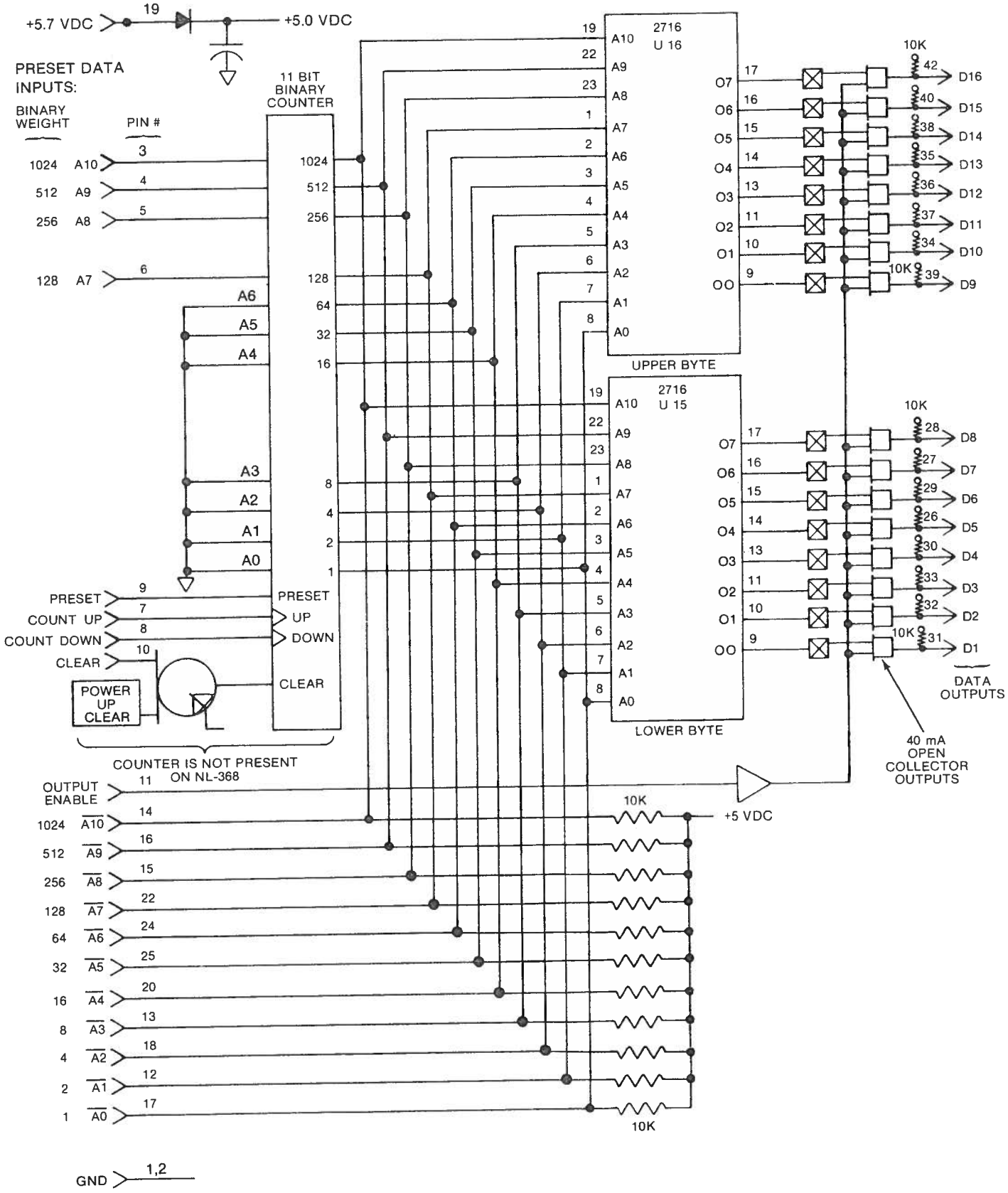
EPROM MODULE

SIMPLIFIED VIEW OF NL-368 MEMORY



EPROM MODULE

SIMPLIFIED SCHEMATIC NL368



EPROM MODULE

SCHEMATIC NOTES:

1. CLEAR — Pin 10 - logic level input, asynchronous, level controlled
   Logic 1 — Address is reset to 0000 regardless of other inputs.
   Logic 0 — Other inputs determine function.
2. PRESET — Pin 9 - logic level input, asynchronous, level controlled
   Logic 1 — Data is transferred from preset inputs to counter outputs.
   NOTE: Only A7 — A10 preset inputs are connected to preset input pins. A0 — A6 preset inputs are tied internally to logic 0.
   Logic 0 — Other inputs determine function.
3. COUNT UP — Pin 7 - logic level input, edge controlled
   Counts up one count on each 0 to 1 transition, when the count down input is at logic 1.
4. COUNT DOWN — Pin 8 - logic level input, edge controlled
   Counts down one count on each 0 to 1 transition, when the count up input is at logic 1.
5. PRESET DATA — A7 — A10 - logic level inputs
   Preset data inputs provide a means to enter data into the counter when the preset input is at logic 1. See Truth Table for preset data inputs.

APPLICATION NOTES:

1. The address inputs $\overline{A0}$ — $\overline{A10}$ have no propagation delay in order to allow the EPROMS to operate at full rated speed, if so desired.
2. The NL-368 module uses two model 2716 (2K x 8) EPROM chips as the memory elements. It has 2048 storage (memory) locations. Each location can store any 16-bit binary data pattern and is identified by a unique storage location number. These location numbers (location 0000-2047) are also called memory addresses or step numbers.
3. The NL-368 module is not able to store (write) bit patterns in the memory elements. It can only retrieve (read) bit patterns already stored.
4. To write the bit patterns, the memory elements are removed from the NL-368 module and programmed by an EPROM programmer designed for use with 2716 EPROM chips. Factory programming is also available.
5. The bit patterns are read by specifying the location number (memory address) of the desired pattern. The NL-368 module continuously transfers a copy of the information stored in the specified location number to the data outputs as long as the enable input is at logic 1. If the enable input is at logic 0, all data outputs will be at logic 0.

   The memory address can be generated from either of two sources.
   A. From the on-board presettable up/down counter using the NL-368A module.
   B. From another module via the address inputs when using the NL-368 module without a counter.
6. Pins A0 — A10 are directly connected to the address input pins of the EPROM chips and therefore are used as the address inputs. They are binary logic level inputs. Refer to the table for address inputs on page G17 for further information. Please note that the logic level inputs for the EPROM chips are the inverse of the 300 Series logic levels (i.e. logic 1 = 2.5 - 5.0 VDC and logic 0 = 0.0 - 0.8 VDC).

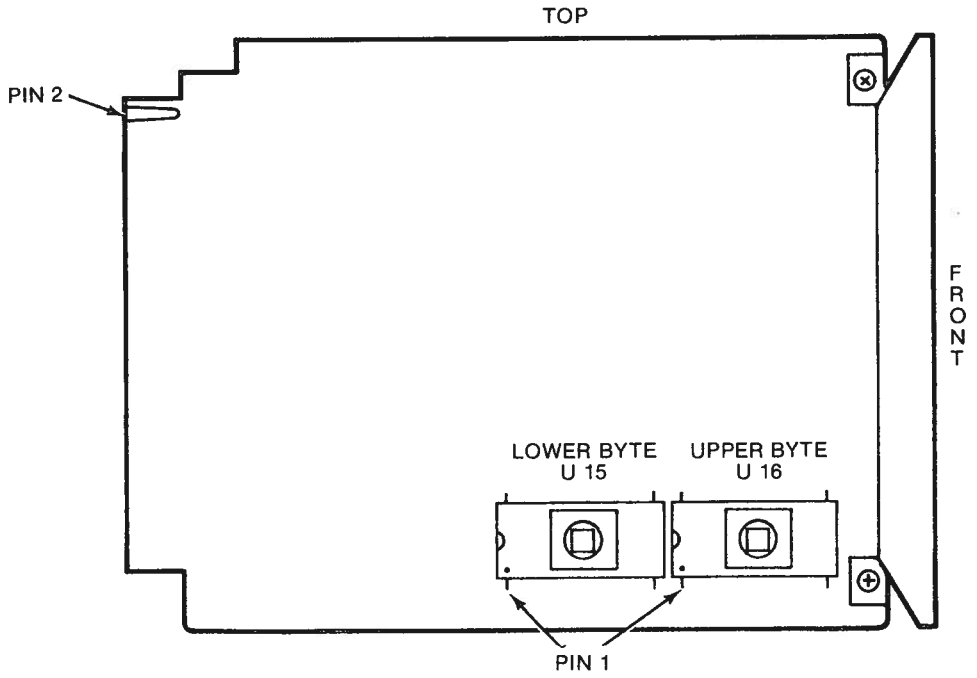
APPLICATION NOTES (CONT'D):

7. The NL-368 module inverts the outputs from the 2716 EPROM chip to 300 Series logic levels. Therefore, if the logic level at the output pin of the EPROM chip is a logic 1 (2.4 - 5.0 VDC) the output pin of the NL-368 module will be at 300 Series logic 1 (0.0 - 0.8 VDC).
8. To prepare for programming the 2716 EPROM chips, a program code must be generated and formatted. Generating the program code involves defining a bit pattern for each memory location. Use the program code sheet on page G22 to help define the bit patterns. Fill in each memory location slot with the bit pattern, using 1 to represent an on state and 0 to represent an off state. After generating the program code, translate the code into the particular format that your programming equipment requires.

   The NL-368 module forms its 16-bit location by using one 8-bit location from each 2716 EPROM chip. This requires one set of input documents for each EPROM chip.
9. Before programming the 2716 EPROM chips, identify each chip to ensure its proper location on the NL-368 module. To do so, place an opaque label over the window on the top of the EPROM chip. Specify on the label which EPROM chip is the upper byte (U16) and which is the lower byte (U15) and the module number, if the system has more than one module.

   The label also protects the memory from accidental erasure. The EPROM chips can be accidentally erased by flourescent light in approximately three years or by sunlight in approximately one week.
10. Erasing the 2716 EPROM chips is not selective. Erasing changes all bits in the memory to a logic 1 (2.4 - 5.0 VDC for the output of the EPROM chip, and 0.0-0.8 VDC for the output of the NL-368 module). Programming can change a bit from a 1 to a 0, but only erasing can change a bit from a 0 to a 1. Erasing is accomplished by exposing the EPROM chip to a source of ultraviolet light. Follow the manufacturers specifications for erasing the EPROM chips.

LOCATION OF 2716 EPROM CHIPS



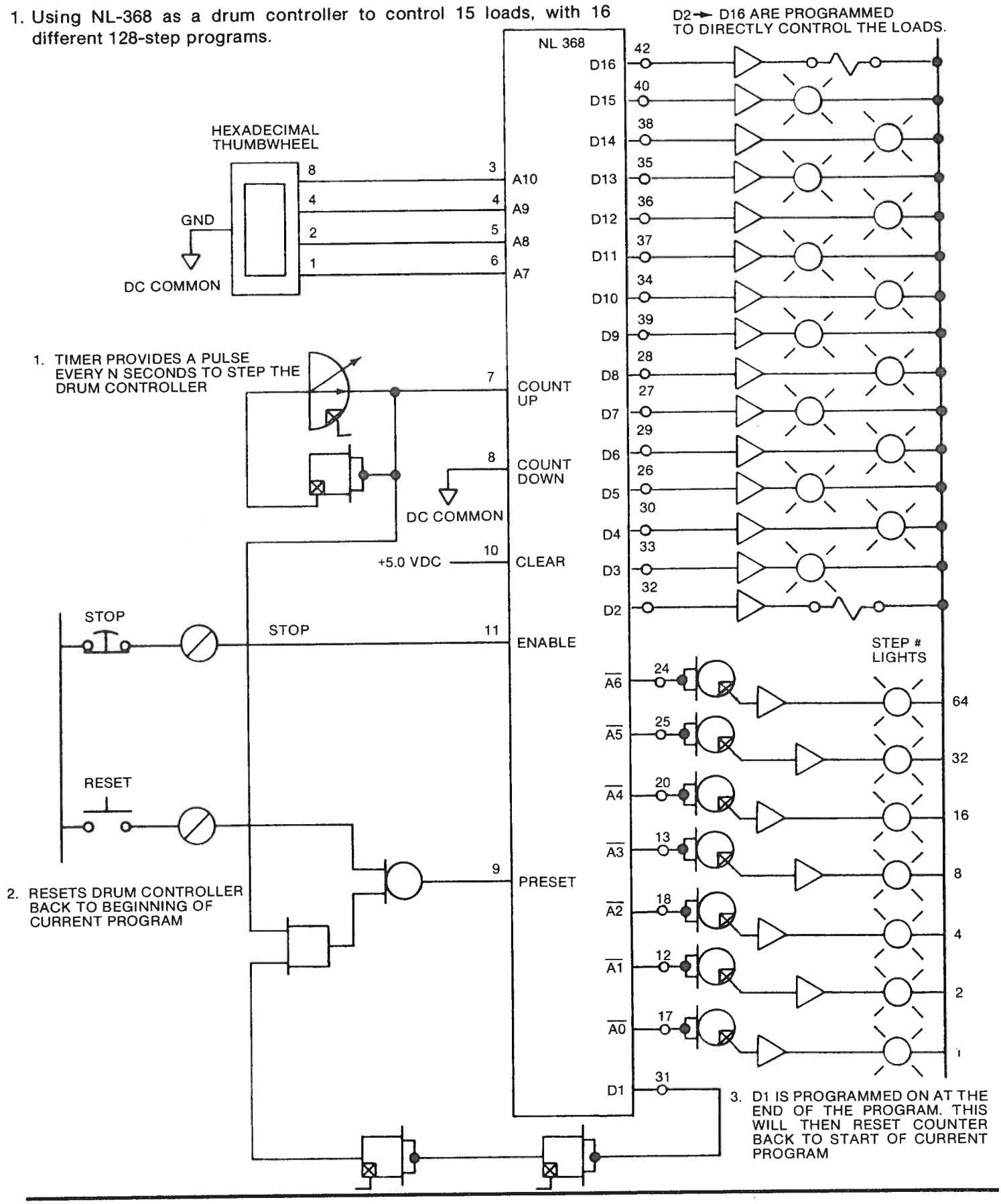
EPROM MODULE

PROGRAM CODE SHEET

2716 Chip Label	U16 Upper Byte								U15 Lower Byte							
2716 Bit Labels	07	06	05	04	03	02	01	00	07	06	05	04	03	02	01	00
2716 Pin #	17	16	15	14	13	11	10	09	17	16	15	14	13	11	10	09
NL-368 Pin #	42	40	38	35	36	37	34	39	28	27	29	26	30	33	32	31
NL-368 Bit Labels	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
Storage Location Number																
0 0 0 0 0 0 0 1 ↓ 2 0 4 7																

APPLICATION EXAMPLES:

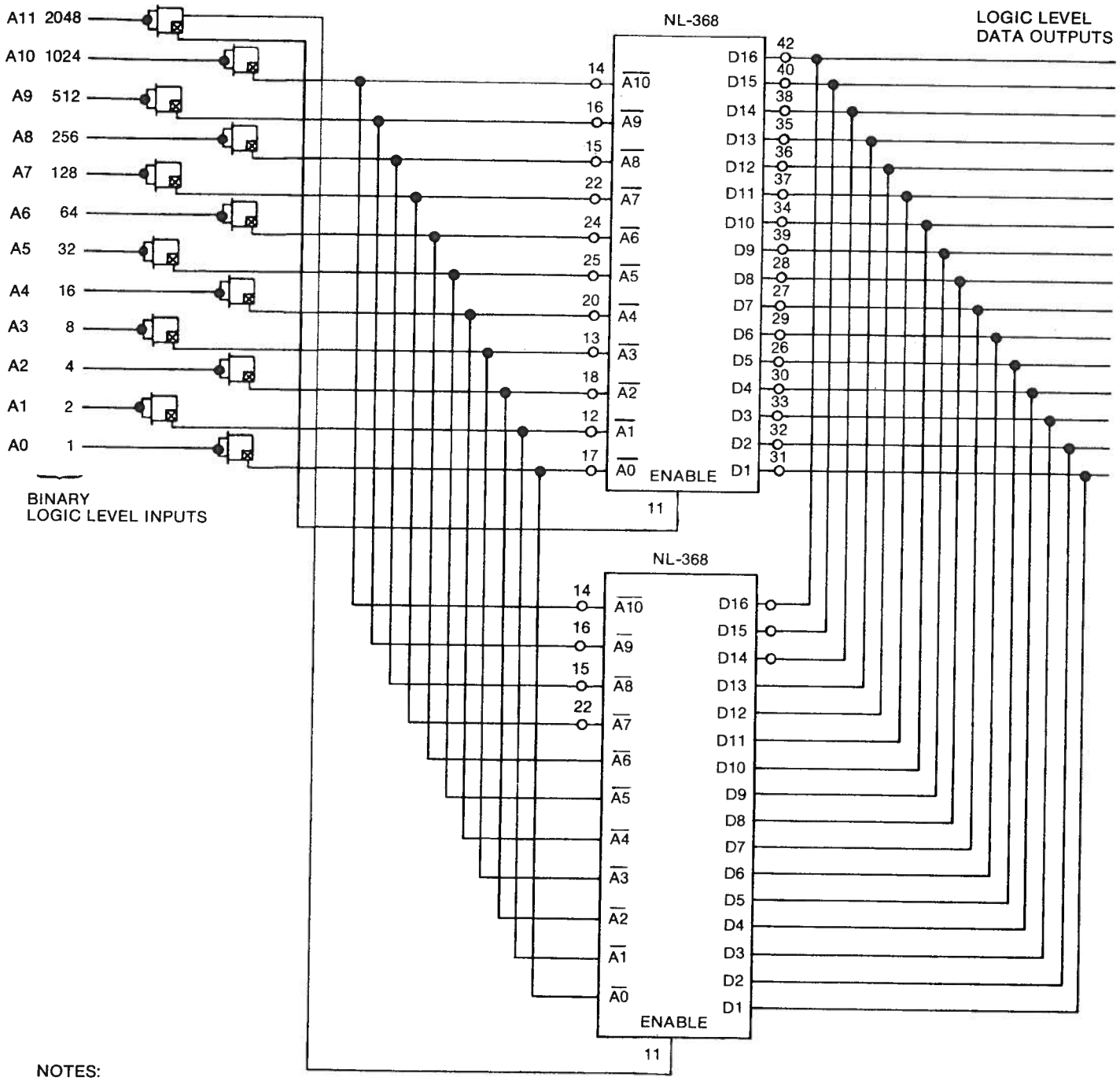
1. Using NL-368 as a drum controller to control 15 loads, with 16 different 128-step programs.



EPROM MODULE

APPLICATION EXAMPLES (CONT'D)

2. Using multiple NL-368 cards to form a larger memory.



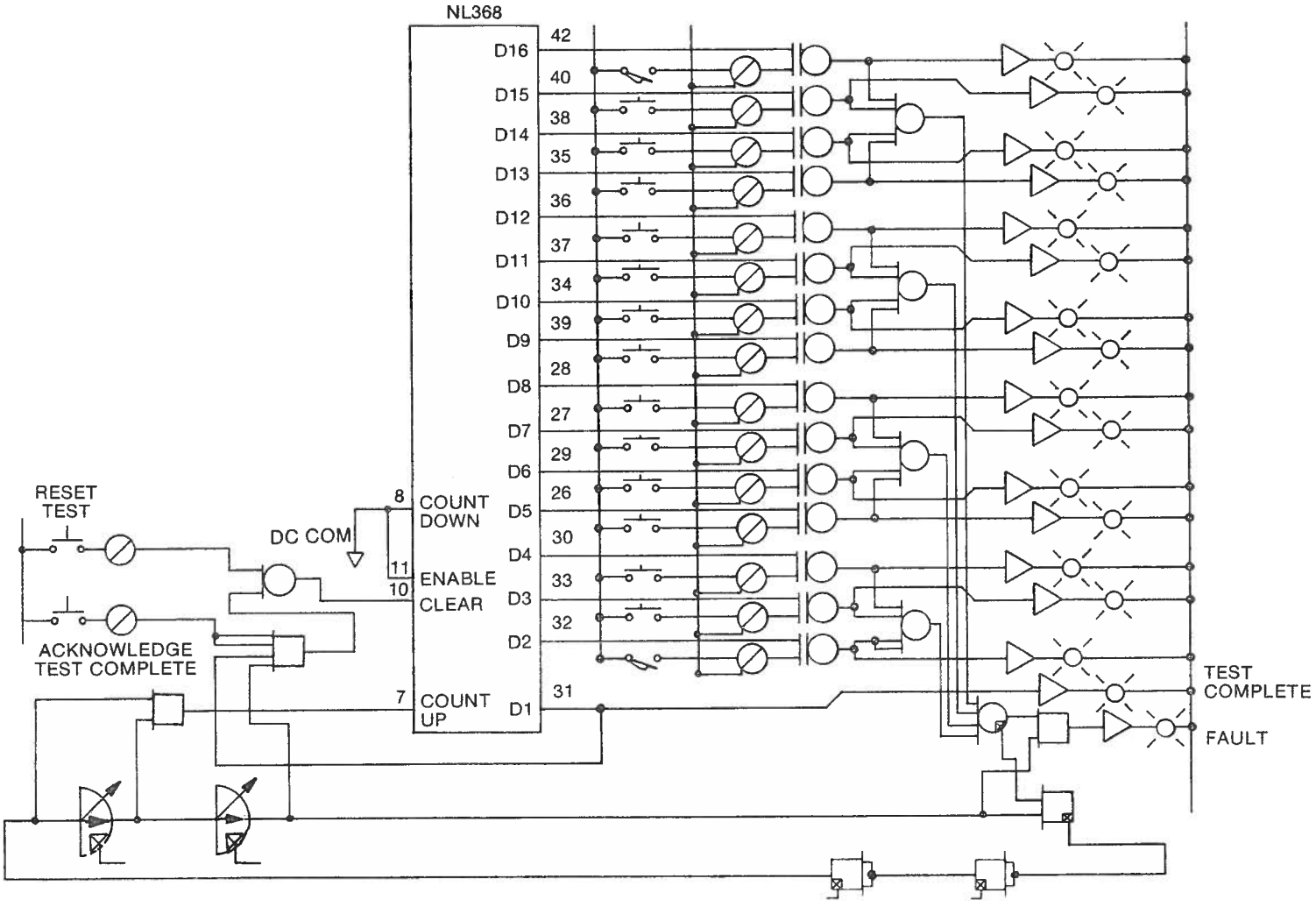
NOTES:

1. ADDRESS LINES HIGHER THAN A10 ARE DECODED TO PROVIDE ONE ENABLE LINE FOR EACH 2K SEGMENT OF MEMORY. ONE NL-368 CAN BE PROGRAMMED TO PROVIDE SELECT LINES FOR 16 ADDITIONAL NL-368 MODULES INSTEAD OF USING 16, 4-INPUT AND MODULES.
2. UP TO 10 NL-368 MODULES CAN BE CONNECTED IN THIS MANNER. WHEN USING NL-325L BUFFERS TO DRIVE THE ADDRESS LINES, UP TO 48 NL-368 MODULES CAN BE CONNECTED TOGETHER, KEEPING THE FAN-OUT AT 10 UNIT LOADS.
3. THE ENABLE INPUT HAS A 3ms PROPAGATION DELAY. THE ADDRESS INPUTS HAVE A 1ms (NOMINAL) PROPAGATION DELAY.

APPLICATION EXAMPLES (CONT'D)

3. Using the NL-368 module as a programmable self-diagnosing test sequence or control sequence generator.

   One NL-368 stores a series of test (output) patterns (not shown). Another NL-368 stores the series of correct responses to the generating patterns. The exclusive OR compares the state of each input with the desired correct state. When all inputs are correct, the timer times out, the counter is incremented, and the next pattern is checked. If all inputs do not match when the timer times out, a fault light turns on and the inputs that are incorrect will turn on their corresponding lights.



EPROM MODULE

APPLICATION EXAMPLES: (CONT'D)

4. The NL-368 module can also be used to establish look-up tables to:

   A. Linearize an input.

   B. Calculate the solution to an equation.

   C. Find sine, cosine, etc. functions.

   D. Code conversions (ASCII to 16-segment displays; binary to BCD; BCD to binary; binary or BCD to gray, etc.).

   E. Design a custom solid state selector switch.

5. The NL-368 can provide extra memory for:

   A. Off-line storage for programmable controllers.

   B. Off-line storage for other equipment storing:

      1. Programs

      2. Messages for printers or displays

      3. Look-up tables